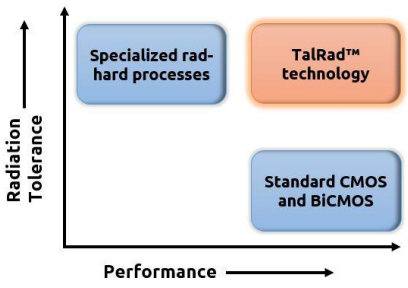
TalRad™ Process Design Kit

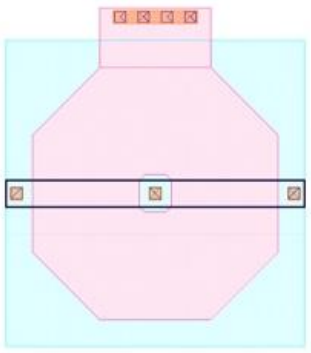
The TalRad™ (**T**ransistor-**a**djusted-**l**ayout for **Rad**iation) PDK, is a rad-hard process design kit with improved total ionizing dose (TID) performance compared to commercial process technologies. The TalRad™ PDK has been implement in TSI Semiconductors' 180nm high voltage CMOS process. Implementing TalRad™ includes the development of design-rule-checker and layout-vs-schematic rule decks, PCELLs and characterizing the radiation performance and reliability of the new components.

The benefits of the TalRad™ PDK:

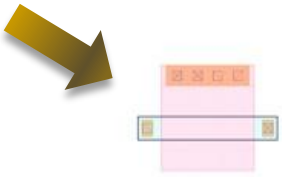
- Up to 10x improvement in TID performance*
- Little to no design size penalty
- Minimal process integration effort
- "Looks and feels" like standard transistor

*compared to the standard PDK components





Example of a 4µm length, minimum width Annular



Comparable TalRad™ (right) transistors shows over a 5x reduction in size

The TalRad™ PDK includes:

- **Annular 1.8V and 5V Transistors**
  - Enclosed gate transistors that reduce the total ionizing dose (TID) induced leakage in the field oxide region of MOSFETs
  - Great for 300krad(Si) applications
- **TalRad™ 1.8V and 5V Transistors**
  - Modified transistors that reduce the TID induced leakage with minimal size impact compared to annular transistors
  - Reduced size and capacitance and improved performance compared to annular transistors
  - Great for precision analog applications
  - Lower quiescent current
  - 75krad(Si) radiation tolerance
  - Radiation performance can be increased for more demanding applications
- **TalRad™ ESD Cells**
  - Class II 4kV ESD, 300krad(Si) radiation tolerance
- Roadmap devices and PDK improvements as they become available
  - TID resilient 50V laterally-diffused MOSFET (LDMOS)
  - 100-150 krad(Si) capable TalRad™ transistors
  - 3.3V annular and TalRad™ transistors

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