# Radiation Hardened Dual D Flip Flop

with **DICE latches** and **cold sparing**

## 1 GENERAL DESCRIPTION

The **AP54RHC705** is a radiation-hardened by design **dual D flip flop** that is ideally suited for space, medical imaging and other applications demanding radiation tolerance and high reliability. It is fabricated in a 180 nm CMOS process utilizing proprietary radiation-hardening techniques, delivering high resiliency to single-event effects (SEE) and to a total ionizing dose (TID) up to 30 krad (Si).

This device is a member of the Apogee Semiconductor AP54RHC logic family operating across a voltage supply range of **1.65 V to 5.5 V**.

This device consists of two D flip-flops with individual clear and clock inputs. Information at a D input is transferred to the corresponding Q output on the next positive-going edge of the clock input. Both Q and $\overline{Q}$ outputs are available for each flip-flop. The clear input is asynchronous.

Zero-power penalty™ cold-sparing is supported, along with Class 2 ESD protection on all inputs and outputs. A proprietary output stage and robust power-on reset (POR) circuit allow the AP54RHC705 to be cold-spared in any redundant configuration with no static power loss on any pad of the device. The redundant output stage also features a high drive capability with low static power loss.

The AP54RHC705 is dual radiation hardened D Flip Flop capable of being clocked up to 100MHz at 3.3V. This device contains latches based on the Dual Interlocked storage Cells (DICE) that are tolerant to Single Event Upsets.

The AP54RHC705 also features a triple-redundant design throughout its entire circuitry, which allows it to be immune to single-event transients (SET) without requiring additional redundant devices.

Ordering information may be found in Table 11 on Page 13.

### 1.1 FEATURES

- **1.65 VDC to 5.5 VDC** operation
- Extended operating temperature range (-55 °C to +125 °C)
- Inputs tolerant up to 5.5 V DC at any $V_{CC}$
- Tri-state output drivers
- Proprietary **cold-sparing capability** with **zero** static power penalty
- **Built-in triple redundancy** for enhanced reliability
- Internal power-on reset (POR) circuitry ensures reliable power up and power down responses during hot plug and cold sparing operations
- Class 2 ESD protection (4000 V HBM, 500 V CDM)
- TID resilience of **30 krad (Si)**
- SEL resilient up to LET of **80 MeV-cm²/mg**

### 1.2 LOGIC DIAGRAM

The AP54RHC705 block diagram is shown below:

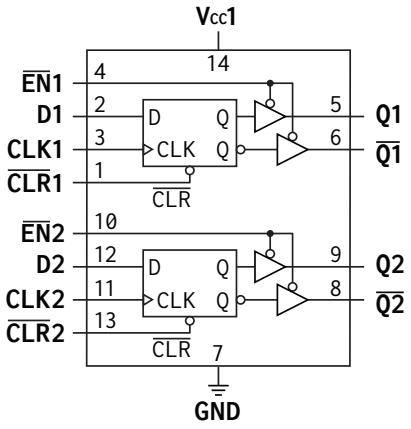


**Figure 1:** AP54RHC705 block diagram

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# 2 ACRONYMS AND ABBREVIATIONS

| | |
|---|---|
| ESD | Electrostatic Discharge |
| POR | Power On Reset |
| RHA | Radiation Hardness Assurance |
| SEE | Single Event Effects |
| SEL | Single Event Latchup |
| SET | Single Event Transient |
| TID | Total Ionizing Dose |
| TMR | Triple Modular Redundancy |
| CDM | Charged-device Model |
| HBM | Human-body Model |

# 3 LOGIC DATA

## 3.1 TRUTH TABLE

The AP54RHC705 truth table is found in Table 1. **H** indicates HIGH logic level, **L** indicates LOW logic level, and **X** indicates DON'T CARE for each flip-flop. $\mathbf{Q_0}$ is stored value in device.

| Input | | | | Internal FF | Output | |
|---|---|---|---|---|---|---|
| $\overline{EN}$ | $\overline{CLR}$ | CLK | D | $Q_{INT}$ | Q | $\overline{Q}$ |
| H | L | X | X | L | Z | Z |
| H | H | ↑ | H | H | Z | Z |
| H | H | ↑ | L | L | Z | Z |
| H | H | H, L or ↓ | X | No Change | Z | Z |
| L | L | X | X | L | $Q_{INT}$ | $\overline{Q_{INT}}$ |
| L | H | ↑ | H | H | $Q_{INT}$ | $\overline{Q_{INT}}$ |
| L | H | ↑ | L | L | $Q_{INT}$ | $\overline{Q_{INT}}$ |
| L | H | H, L or ↓ | X | No Change | $Q_{INT}$ | $\overline{Q_{INT}}$ |

**Table 1:** AP54RHC705 device truth table (per gate).

# 4 PIN CONFIGURATION

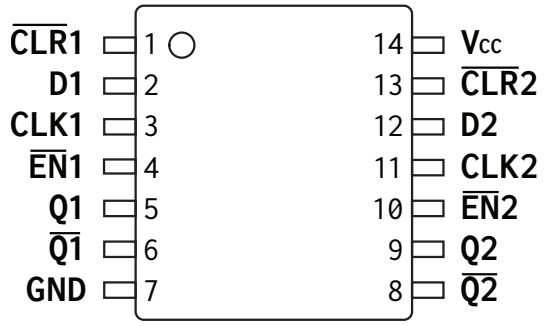



**Figure 2:** AP54RHC705 Device Pinout.

**Table 2:** AP54RHC705 device pinout description

| PIN NAME(S) | PIN NUMBER(S) | DESCRIPTION |
|---|---|---|
| $\overline{CLR1}$, $\overline{CLR2}$ | 1, 13 | Asynchronous Clears |
| D1, D2 | 2, 12 | Data Inputs |
| Q1, Q2 | 5, 9 | Outputs |
| $\overline{Q1}$, $\overline{Q2}$ | 6, 8 | Complementary Outputs |
| $\overline{EN1}$, $\overline{EN2}$ | 4, 10 | Output Enables |
| $V_{CC}$ | 14 | Positive Voltage Supply |
| GND | 7 | Ground |

# 5 ELECTRICAL CHARACTERISTICS

The sign convention for current follows JEDEC standards with negative values representing current sourced from the device and positive values representing current sunk into the device.

## 5.1 ABSOLUTE MAXIMUM RATINGS

Excursions beyond the values listed in Table 3 may cause permanent damage to the device. Proper function of the device cannot be guaranteed if these values are exceeded, and long-term device reliability may be affected. Functionality of the device at these values, or beyond those listed in Recommended Operating Conditions (Table 4) is not guaranteed.

All parameters are specified across the entire operating temperature range unless otherwise specified.

**Table 3:** Absolute Maximum Ratings

| SYMBOL | PARAMETER | | VALUE | UNITS |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | -0.5 to +5.5 | V |
| $V_I$ | Input voltage range | | -0.5 to +5.5 | V |
| $V_O$ | Output voltage range | | -0.5 to $V_{CC}$ + 0.5 (1) | V |
| $I_{IK}$ ($V_I$ < 0) | Input clamp current | | 100 | mA |
| $I_O$ | Continuous output current (per pin) | | 100 | mA |
| $I_{CC}$ | Maximum supply current | | 100 | mA |
| $V_{ESD}$ | ESD Voltage | HBM | 4000 | V |
| | | CDM | 500 | V |
| $T_J$ | Operating junction temperature range | | -55 to +150 | °C |
| $T_{STG}$ | Storage temperature range | | -65 to +150 | °C |

(1) $V_O$ must remain below absolute maximum rating of $V_{CC}$

## 5.2 RECOMMENDED OPERATING CONDITIONS

All recommended parameters below are specified across the entire operating temperature range unless otherwise specified.

**Table 4:** Recommended Operating Conditions

| SYMBOL | PARAMETER | | MIN | MAX | UNITS |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 1.65 | 5.5 | V |
| $V_I$ | Input voltage range | | 0 | 5.5 | V |
| $V_O$ | Output voltage range | | 0 | $V_{CC}$ | V |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 1.65 to 1.95 V | 1.4 | - | V |
| | | $V_{CC}$ = 2.3 to 2.7 V | 1.9 | - | |
| | | $V_{CC}$ = 3.0 to 3.6 V | 2.5 | - | |
| | | $V_{CC}$ = 4.5 to 5.5 V | 3.8 | - | |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 1.65 to 1.95 V | - | 0.4 | V |
| | | $V_{CC}$ = 2.3 to 2.7 V | - | 0.6 | |
| | | $V_{CC}$ = 3.0 to 3.6 V | - | 0.9 | |
| | | $V_{CC}$ = 4.5 to 5.5 V | - | 1.35 | |
| $I_{OH}$ | HIGH-level output current | $V_{CC}$ = 1.65 to 1.95 V | - | -4 | mA |
| | | $V_{CC}$ = 2.3 to 2.7 V | - | -8 | |
| | | $V_{CC}$ = 3.0 to 3.6 V | - | -16 | |
| | | $V_{CC}$ = 4.5 to 5.5 V | - | -24 | |
| $I_{OL}$ | LOW-level output current | $V_{CC}$ = 1.65 to 1.95 V | - | 4 | mA |
| | | $V_{CC}$ = 2.3 to 2.7 V | - | 8 | |
| | | $V_{CC}$ = 3.0 to 3.6 V | - | 16 | |
| | | $V_{CC}$ = 4.5 to 5.5 V | - | 24 | |
| $t_r$, $t_f$ | Input rise or fall time (10% - 90%) | $V_{CC}$ = 1.65 to 1.95 V | - | 1000 | ns |
| | | $V_{CC}$ = 2.3 to 2.7 V | - | 600 | |
| | | $V_{CC}$ = 3.0 to 3.6 V | - | 500 | |
| | | $V_{CC}$ = 4.5 to 5.5 V | - | 400 | |

**Table 5:** Thermal Information

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $T_J$ | Operating junction temperature | -55 | - | +125 | °C |
| $R_{\theta JA}$ | Junction to ambient thermal resistance | - | 100 | - | °C/W |

## 5.3 STATIC CHARACTERISTICS

All parameters are specified across the entire operating temperature range unless otherwise specified.

**Table 6:** DC Electrical Characteristics

| SYMBOL | PARAMETER | CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{OL}$ | LOW-level output voltage | $I_O$ = 100 µA | 1.65 to 5.5 V | - | 0.02 | 0.05 | V |
| | | $I_O$ = 1 mA | 1.65 to 5.5 V | - | 0.05 | 0.1 | V |
| | | $I_O$ = 4 mA | 2.3 V | - | 0.3 | 0.6 | V |
| | | | 3.0 V | - | 0.2 | 0.4 | V |
| | | | 4.5 V | - | 0.2 | 0.4 | V |
| | | $I_O$ = 8 mA | 2.3 V | - | 0.6 | 1.0 | V |
| | | | 3.0 V | - | 0.4 | 0.8 | V |
| | | | 4.5 V | - | 0.3 | 0.6 | V |
| | | $I_O$ = 16 mA | 3.0 V | - | 1.0 | 1.4 | V |
| | | | 4.5 V | - | 1.1 | 1.5 | V |
| | | $I_O$ = 24 mA | 4.5 V | - | 1.1 | 1.5 | V |
| $V_{OH}$ | HIGH-level output voltage | $I_O$ = -100 µA | 1.65 to 5.5 V | $V_{CC}$ - 0.1 | $V_{CC}$ - 0.02 | - | V |
| | | $I_O$ = -1 mA | 1.65 to 5.5 V | $V_{CC}$ - 0.15 | $V_{CC}$ - 0.08 | - | V |
| | | $I_O$ = -4 mA | 2.3 V | 1.8 | 2.0 | - | V |
| | | | 3.0 V | 2.6 | 2.8 | - | V |
| | | | 4.5 V | 4.2 | 4.4 | - | V |
| | | $I_O$ = -8 mA | 2.3 V | 1.4 | 1.7 | - | V |
| | | | 3.0 V | 2.2 | 2.5 | - | V |
| | | | 4.5 V | 3.9 | 4.1 | - | V |
| | | $I_O$ = -16 mA | 3.0 V | 1.5 | 2.0 | - | V |
| | | | 4.5 V | 3.3 | 3.8 | - | V |
| | | $I_O$ = -24 mA | 4.5 V | 3.0 | 3.5 | - | V |
| $I_{CC}$ | Quiescent supply current | $V_I$ = $V_{CC}$ or GND<br>$I_O$ = 0 mA | 5.5 V | - | 56 | 205 | µA |
| $I_I$ | Input current | $V_I$ = $V_{CC}$ or GND | 1.65 to 5.5 V | - | - | ±1 | µA |
| $I_{OFF}$ | Powerdown leakage current(1) | $V_I$ = $V_{CC}$ or GND | OFF(2) | - | - | 5 | µA |

(1) into any input or output port
(2) $V_{CC}$ is disconnected or at GND potential

## 5.4 DYNAMIC CHARACTERISTICS

All parameters are specified across the entire operating temperature range unless otherwise specified.

### 5.4.1 Timing Requirements

**Table 7:** Timing Requirements

| SYMBOL | PARAMETER | CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $t_{su}$ | Setup Time (Data to Clock) | $C_L$ = 50 pF | 4.5 to 5.5 V | TBD | 5.7 | - | ns |
| | | | 3.0 to 3.6 V | TBD | 6.7 | - | ns |
| | | | 2.3 to 2.7 V | TBD | 8.5 | - | ns |
| | | | 1.65 to 1.95 V | TBD | 13.5 | - | ns |
| $t_h$ | Hold Time (Clock to Data **Q**, $\overline{\mathbf{Q}}$) | $C_L$ = 50 pF | 4.5 to 5.5 V | TBD | 0.9 | - | ns |
| | | | 3.0 to 3.6 V | TBD | 1.4 | - | ns |
| | | | 2.3 to 2.7 V | TBD | 2 | - | ns |
| | | | 1.65 to 1.95 V | TBD | 3.4 | - | ns |
| $t_w$ | Pulse Width (Clock) | $C_L$ = 50 pF | 4.5 to 5.5 V | TBD | 3.6 | - | ns |
| | | | 3.0 to 3.6 V | TBD | 4.1 | - | ns |
| | | | 2.3 to 2.7 V | TBD | 4.9 | - | ns |
| | | | 1.65 to 1.95 V | TBD | 7.2 | - | ns |
| $f_{max}$ | Clock Frequency (50% Duty Cycle) | $C_L$ = 50 pF | 4.5 to 5.5 V | - | - | TBD | MHz |
| | | | 3.0 to 3.6 V | - | - | TBD | MHz |
| | | | 2.3 to 2.7 V | - | - | TBD | MHz |
| | | | 1.65 to 1.95 V | - | - | TBD | MHz |

### 5.4.2 Operating Characteristics

**Table 8:** Operating Characteristics

| SYMBOL | PARAMETER | CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_I$ = $V_{CC}$ or GND | 1.65 to 5.5 V | - | 6 | 10 | pF |
| $C_{PD}$ | Power dissipation capacitance | $I_O$ = 0 mA, f = 1 MHz | 5.5 V | - | TBD | - | pF |

### 5.4.3 Switching Characteristics

**Table 9:** Switching Characteristics

| SYMBOL | PARAMETER | CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $t_{pdclk}$ | Propagation Delay (Clock to Data **Q**, $\overline{\mathbf{Q}}$) | $C_L$ = 50 pF | 4.5 to 5.5 V | - | 16 | TBD | ns |
| | | | 3.0 to 3.6 V | - | 20 | TBD | ns |
| | | | 2.3 to 2.7 V | - | 24 | TBD | ns |
| | | | 1.65 to 1.95 V | - | 35 | TBD | ns |
| $t_{pdclr}$ | Propagation Delay ($\overline{CLR}$ to **Q**, $\overline{\mathbf{Q}}$) | $C_L$ = 50 pF | 4.5 to 5.5 V | - | 21 | TBD | ns |
| | | | 3.0 to 3.6 V | - | 27 | TBD | ns |
| | | | 2.3 to 2.7 V | - | 33 | TBD | ns |
| | | | 1.65 to 1.95 V | - | 50 | TBD | ns |
| $t_{tlh, thl}$ | Output Transition Time | $C_L$ = 50 pF | 4.5 to 5.5 V | - | 5.3 | TBD | ns |
| | | | 3.0 to 3.6 V | - | 11.4 | TBD | ns |
| | | | 2.3 to 2.7 V | - | 14.5 | TBD | ns |
| | | | 1.65 to 1.95 V | - | 24.4 | TBD | ns |
| $t_{clr}$ | Pulse Width ($\overline{CLR}$) | $C_L$ = 50 pF | 4.5 to 5.5 V | TBD | 5.8 | - | ns |
| | | | 3.0 to 3.6 V | TBD | 6 | - | ns |
| | | | 2.3 to 2.7 V | TBD | 6.5 | - | ns |
| | | | 1.65 to 1.95 V | TBD | 8.5 | - | ns |
| $t_{en}$ | Output Enable Time ($\overline{EN}$ ↑ to Data **Q**, $\overline{\mathbf{Q}}$) | $C_L$ = 50 pF | 4.5 to 5.5 V | - | 15 | TBD | ns |
| | | | 3.0 to 3.6 V | - | 22 | TBD | ns |
| | | | 2.3 to 2.7 V | - | 29 | TBD | ns |
| | | | 1.65 to 1.95 V | - | 43 | TBD | ns |
| $t_{dis}$ | Output Disable Time ($\overline{EN}$ ↓ to Data **Q**, $\overline{\mathbf{Q}}$) | $C_L$ = 50 pF | 4.5 to 5.5 V | - | 15 | TBD | ns |
| | | | 3.0 to 3.6 V | - | 22 | TBD | ns |
| | | | 2.3 to 2.7 V | - | 29 | TBD | ns |
| | | | 1.65 to 1.95 V | - | 43 | TBD | ns |

## 5.5 RADIATION RESILIENCE

For detailed radiation testing reports, please contact Apogee Semiconductor at sales@apogeesemi.com.

**Table 10:** Radiation Resilience Characteristics

| PARAMETER | CONDITIONS | VALUE | UNITS |
|---|---|---|---|
| Total Ionizing Dose (TID) | Please contact Apogee Semiconductor for test report. | 30 | krad (Si) |
| SEE LET Threshold | Please contact Apogee Semiconductor for test report. | <80 | MeV-cm$^2$/mg |

## 5.6 CHARACTERISTICS MEASUREMENT INFORMATION

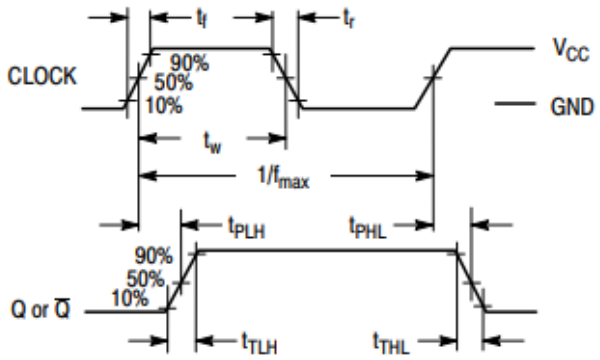



**Figure 3:** Timing measurements

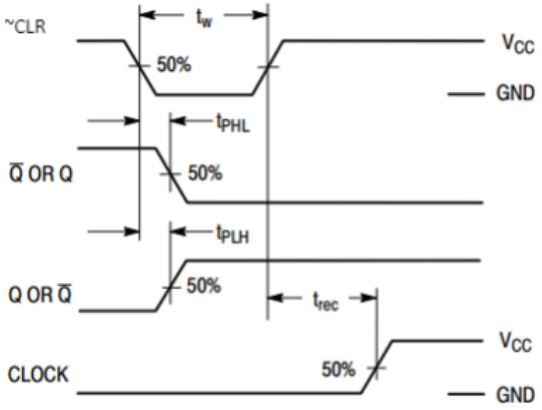



**Figure 4:** Propagation delay measurement

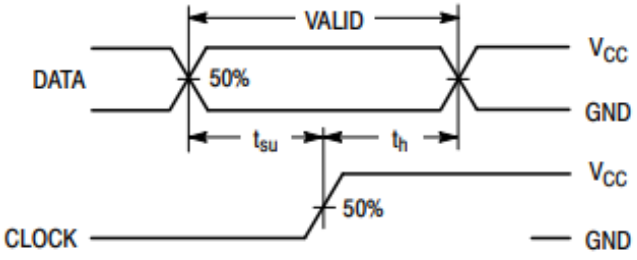



**Figure 5:** Setup and hold time measurement

# 6 DETAILED DESCRIPTION

The AP54RHC705 is a dual D flip flop designed to operate from a wide supply voltage of 1.65 to 5.5 V with fully redundant input and output stages, providing for superior radiation resilience.

The output and input stages are constructed with transient activated clamps (Figure 6, 7) that prevent inadvertent biasing of the $V_{CC}$ power rail through parasitic diodes inherent to conventional input, output, and ESD circuits. The IC also incorporates an internal power-on reset (POR) circuit that prevents the output from driving erroneous results during power-on, and guarantees correct operation at power supply voltages as low as 1.65 V. While the supply is ramping, the POR holds the output buffer in tri-state, a feature that prevents unwanted DC current during cold sparing on input and output pins.

The AP54RHC family's I/O protection circuitry allows for cold sparing configurations as it avoids a leakage current penalty on inputs and outputs while in a power-down state. This can result in considerable power savings in systems where multiple-path redundancy is employed. The ESD clamp circuits for this logic family are designed to support Class 2 ESD levels of 4 kV HBM and 500 V CDM.

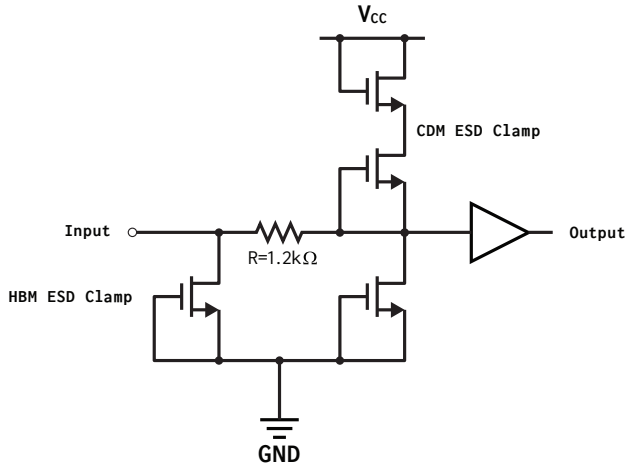



**Figure 6:** Details of input pin structure

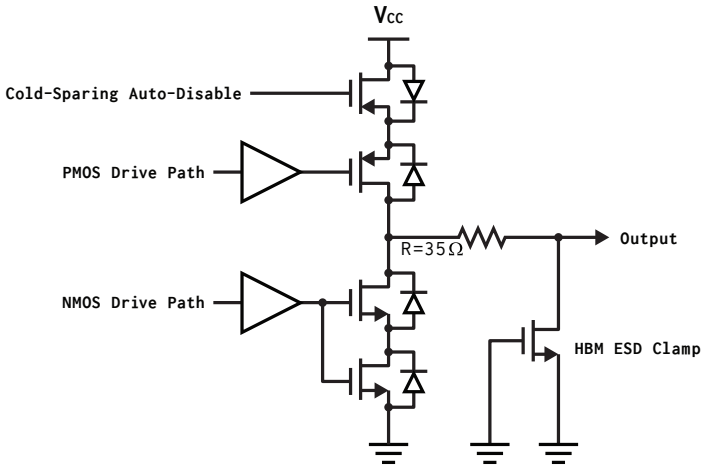



**Figure 7:** Details of output pin structure

**Note**

During tri-state, the application must ensure that the output pins are either held or switched to logic high or logic low levels i.e. close to **$V_{CC}$** or **GND**, otherwise increased supply current can occur.

# 7 APPLICATIONS INFORMATION

## 7.1 USE IN COLD-SPARING CONFIGURATION

As the AP54RHC family is radiation-hardened by design and includes internal TMR, it can be utilized in high-reliablity applications without additional supporting circuitry or devices. Nonetheless, some application requirements call for fully-redundant designs, where an “A” and a “B” device are required, often on separate power rails.

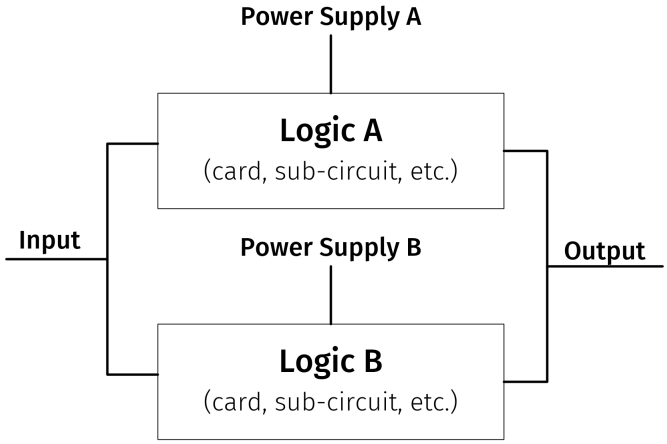



**Figure 8:** Two-path cold-sparing configuration.

With the cold-sparing capability of the AP54RHC family, fully redundant “A” and “B” functions may be placed in parallel (as seen in Figure 8) running off redundant power supplies. The inputs and outputs on each one of these functions are assumed to be based on the AP54RHC family, allowing for direct parallel connection without unwanted leakage current paths during cold sparing. In the event of a failure in power supply A or within function A, the system can simply shut power supply A off and switch on power supply B, without requiring additional input or output switching or configuration changes.

## 7.2 POWER SUPPLY RECOMMENDATIONS

This device can operate at any voltage within the range specified in Table 4 Recommended Operating Conditions.

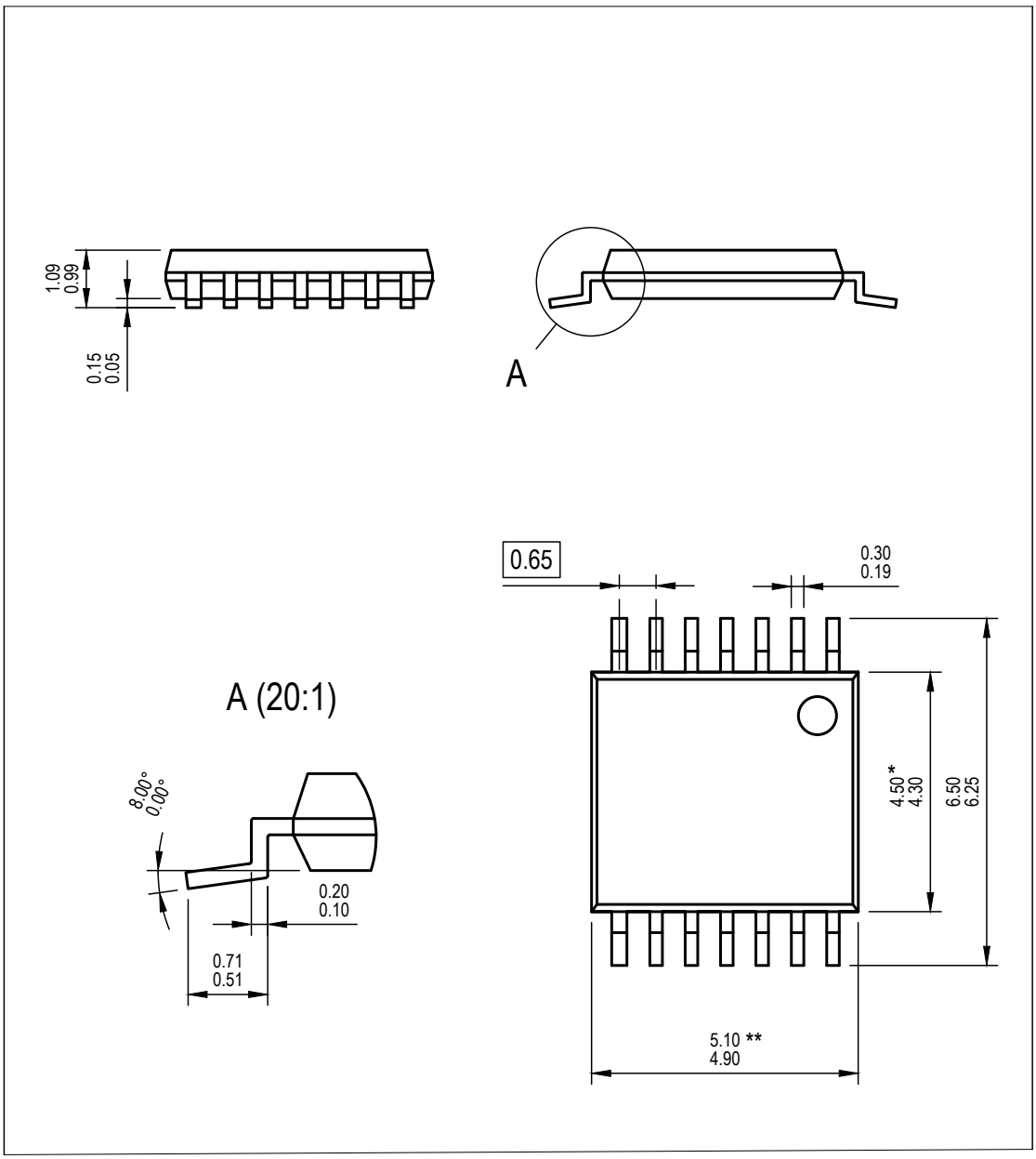
At a minimum, a 16 VDC (or higher), X7R-rated 0.1 µF ceramic decoupling capacitor should be placed near (within 1 cm) the $V_{CC}$ pin of the device.

## 7.3 APPLICATION TIPS

Unused **inputs** must **not** be left floating. They may be connected to either a low (GND) or high ($V_{CC}$) bias to provide a known state at the input of the device. Resistors may be used to tie off unused inputs. In the event of a design change, such resistors can be removed, thereby allowing use of the inputs without having to cut traces on the PCB.

An unused **output** may be left floating. It is suggested that it be routed to a test point or similar accessible structure in case the gate needs to be utilized as part of a design revision.

# 8 PACKAGING INFORMATION




Notes:
1. All linear dimensions are in millimeters. Dimensioning and tolerancing are as per ISO/TS 128-71:2010
2. The part is compliant with JEDEC MO-153 specifications.

* Body width does **not** include interlead flash. Interlead flash shall not exceed 0.25 mm each side.
** Body length does **not** include mold flash, protrusion, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0.15 mm on each side.

**Figure 9:** Package Mechanical Detail

# 9 ORDERING INFORMATION

Example part numbers for the AP54RHC705 are listed in Table 11. The full list of options for this part can be found in Figure 10. Please contact Apogee Semiconductor sales at sales@apogeesemi.com for further information on sampling, lead time and purchasing on specific part numbers.

**Table 11:** AP54RHC705 Ordering Information

| DEVICE | DESCRIPTION | PACKAGE |
|---|---|---|
| AP54RHC705ELT-W | Radiation Hardened Dual D Flip Flop (for evaluation only) | Plastic TSSOP-14 |
| AP54RHC705ALT-T | Radiation Hardened Dual D Flip Flop (30 krad (Si)) | Plastic TSSOP-14 |

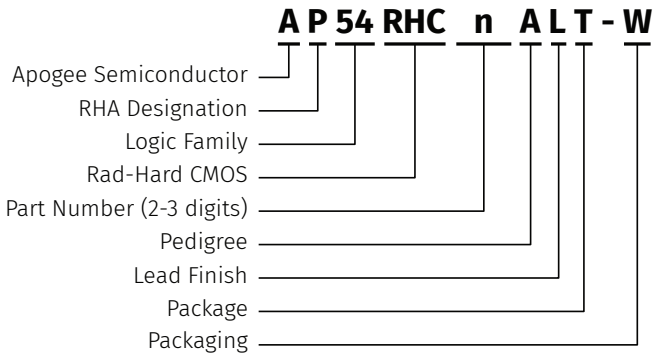



**Figure 10:** Part Number Decoder

1. RHA Designation
   - **P** 30 krad (Si)
2. Part Number
   - **_** 705 (Dual D Flip Flop)
3. Pedigree
   - **A** -55 to +125 °C (Burn-in)
   - **B** -55 to +125 °C (No burn-in)
   - **E** 25 °C Functional Test Only (Evaluation)
4. Lead Finish
   - **L** Tin-Lead (SnPb)
   - **T** Matte Tin (Sn)
5. Package
   - **T** 14-pin Thin Shrink Small Outline Package (TSSOP)
6. Packaging
   - **W** Waffle Pack
   - **J** JEDEC Tray
   - **R** Tape and Reel
   - **T** Tube

# 10 REVISION HISTORY

| REVISION | DESCRIPTION | DATE |
|---|---|---|
| A03 | Updated device description, output structure image and parametric characteristics tables. | 2022-08-25 |
| A02 | Updated formatting and parametric characteristics table. | 2021-07-11 |
| A01 | Initial Release. | 2020-02-29 |

For the latest version of this document, please visit https://www.apogeesemi.com.

# 11 LEGAL

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