

Portfolio Overview



1

7/1/2020

Our Company



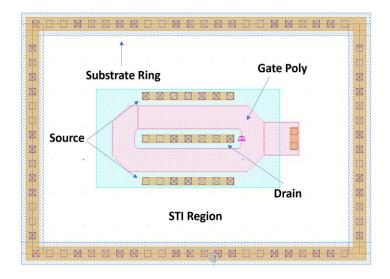
- Enabling small satellite applications by:
 - Bridging the technology gap between commercial and high reliability components
 - Significantly lowering the cost of rad-hard ICs

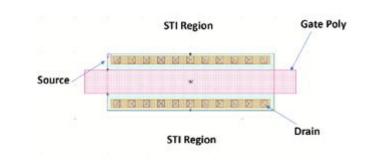
- Focused on Power and Analog rad-hard IC design, IP and process development
- R&D contracts with AFRL, DoE, NSF and NASA
- Growing portfolio
 - 17 products sampling in 2020
 - Expected to double in 2021
- Partnered with a Trusted 180 nm highvoltage CMOS foundry to develop a radhard process (TalRad[™])



The TalRad[™] Rad-Hard PDK includes:

- Annular 1.8V and 5V Transistor
 - Great for greater than 300krad(Si) applications
- TalRad[™] 1.8V and 5V Transistors
 - Reduced size and capacitance and improved performance compared to annular transistors
 - Great for precision analog applications
 - Lower quiescent current
- TalRad[™] ESD Cells
 - Class II 4kV ESD, 300krad(Si) radiation tolerance
- Rad-Hard 1.8V Digital Cell Library
- Roadmap devices and PDK improvements as they become available
- Available in TSI Semiconductors 180nm process

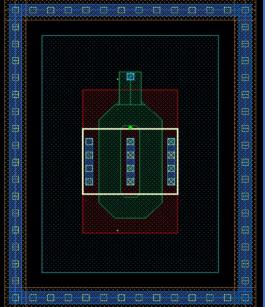






TalRad[™] PDK and PCELLs (Available Now!)

Custom PCELL (Annular)



Create	e Instance	- • ×	
Library	cmhv7sf_apg	Browse	
Cell	BB_annular_NMOS		
View	layout		
Names	I6	Pcell	
	🛃 Halo		
	Define Halo		
	Physical Only		
▼ Mosaic	Create as mosaic		
Rows,Columns	1	1	
Delta Y,X	9.08	7.96	
 Parameters 			
Width	6		
Length	0.7		
PC appendix mode	top		
RX enclosure for CA left	0.2		
RX enclosure for CA right	0.2		
Multiplicity for transistor	1		
	⊻ Enable Bottom ring		
Extend ring down in 0.56um steps	0		
	Enable Top ring		
Extend ring upwards in 0.56um steps			
	Enable Left ring		
Extend ring to Left in 0.56um steps			
Extend ring to Dight in 0.56um steps	Enable Right ring		
Extend ring to Right in 0.56um steps	0		
	Hide	Defaulte	

CUSTOM LVS Deck (TALRAD, Annular, and ESD) Efficiency = Better ICs Errors

CUSTOM DRC Deck (TALRAD and Annular)

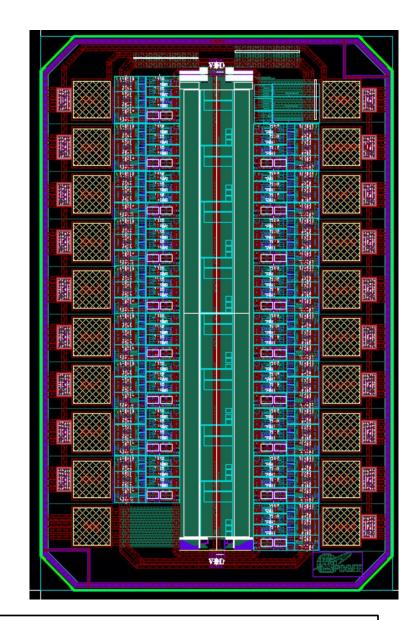
ess

AP54RHCXXX family

Sampling now!

A family of radiation hardened logic gates in plastic packages built with the TalRad[™] PDK:

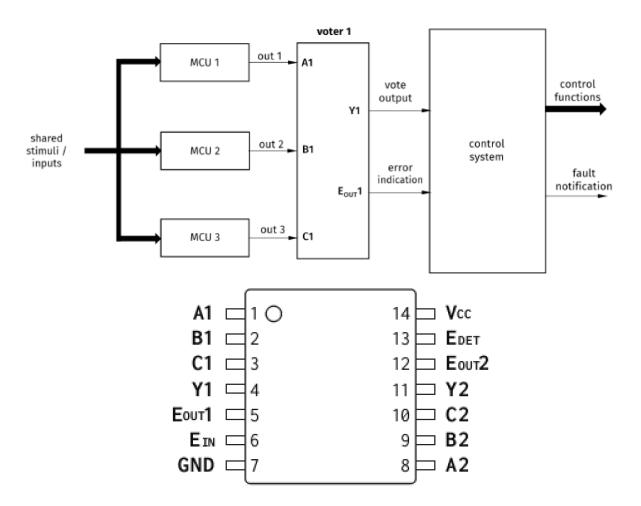
- Industry standard pinout includes a:
 - Two supply level shifter
 - Single supply transceiver
 - Voter with daisy chain error detect
 - Other 7400 series logic functions
- TID/SEL hardened up to 30krad (Si) and 80 MeV-cm²/mg
- Latches are DICE (SEU hardened)
- All parts have cold-spare capability
 - Fail-safe inputs and outputs with no static power penalty
- Designed for Class 2 ESD
- TSSOP package, 14 pin package
- Specified over -55°C to +125°C, 1.6V to 5.5V V_{DD}
- View portfolio at: https://apogeesemi.com/products/





AP54RHC301 – Dual 3-input Majority Voter

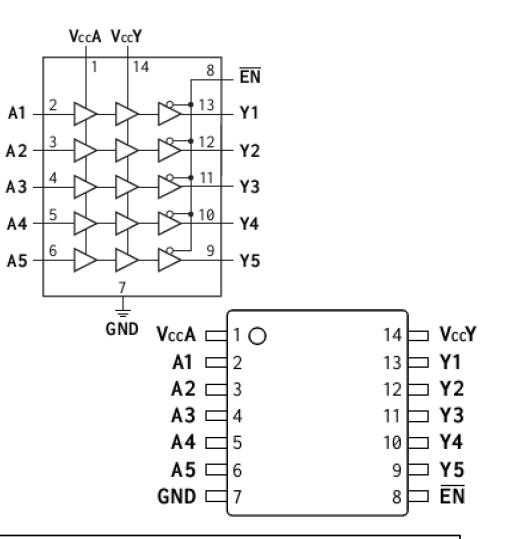
- 1.65 VDC to 5.5 VDC operation
- Provides logic-level down translation to VCC
- Extended operating temperature range
 - (-55 °C to +125 °C)
- Proprietary cold-sparing capability with zero static power penalty
- Built-in triple redundancy
- Internal power-on reset (POR)
- Class 2 ESD protection
 - (4000 V HBM, 500 V CDM)
- TID resilience of 30 krad (Si)
- SEL resilient up to LET of 80 MeV-cm²/mg





AP54RHC504 – 5-Channel Level Translator

- 1.65 VDC to 5.5 VDC operation
- Inputs tolerant up to 5.5 VDC at any $V_{cc}A$ or $V_{cc}Y$
- Extended operating temperature range
 - (-55 °C to +125 °C)
- Proprietary cold-sparing capability with zero static power penalty
- Built-in triple redundancy
- Internal power-on reset (POR)
- Class 2 ESD protection
 - (4000 V HBM, 500 V CDM)
- TID resilience of 30 krad (Si)
- SEL resilient up to LET of 80 MeV-cm²/mg

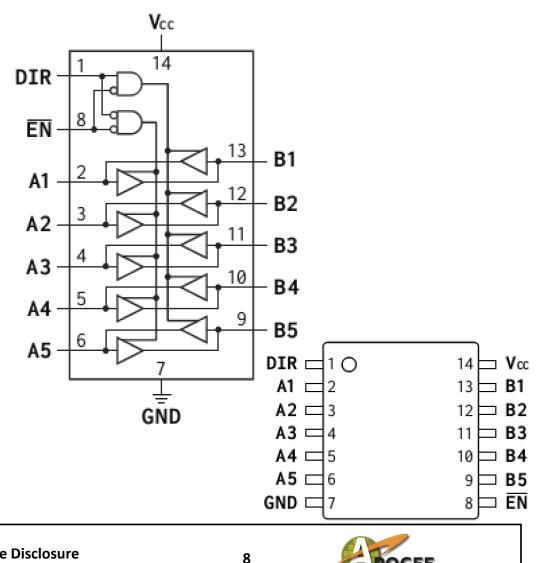




7/1/2020

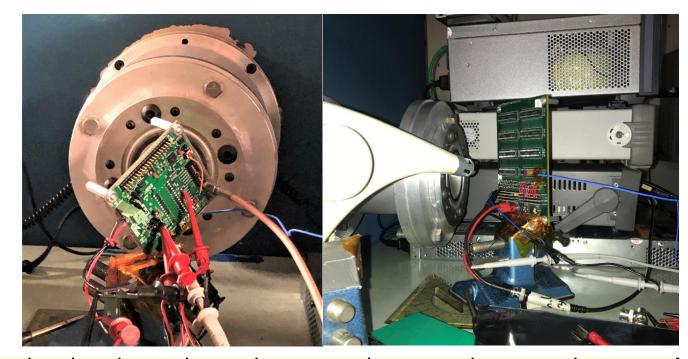
AP54RHC506 – 5-Ch 100MHz Transceiver

- 1.65 VDC to 5.5 VDC operation
- Extended operating temperature range
 - (-55 °C to +125 °C)
- Proprietary cold-sparing capability with zero static power penalty
- Built-in triple redundancy
- Internal power-on reset (POR)
- Class 2 ESD protection
 - (4000 V HBM, 500 V CDM)
- TID resilience of 30 krad (Si)
- SEL resilient up to LET of 80 MeV-cm²/mg



SEE Test Campaign

- Test conducted at LBNL Base Facility
- Testing conducted in air using Xenon
- Angle varied from incident (LET = 55 MeV*cm²/mg) to 45° (LET = 79 MeV*cm²/mg)
- Temperature forcing implemented with hot air gun and remotely monitored with thermo-couple
- NO LATCHUP on any of the runs conducted up to LET 80 T = 100c
- Outputs of IO Cells (High/Low) monitored for perturbations



Unit 1	War	hol T	riple 3	AND (N	Ionitoring 2 IO Outputs Driving High/Low)			
113	Xe	80	25	5	NA	1.00E+04	1.42E+07	Passed
114	Xe	80	100	5	NA	1.00E+04	1.42E+07	Passed
115	Xe	80	100	5.5	NA	1.00E+04	1.42E+07	Passed



Thank You!





