AP54RHC804

Radiation-Hardened 8-Channel Level Translator
with **cold sparing**

1 GENERAL DESCRIPTION

The **AP54RHC804** is a radiation-hardened by design **8-channel level translator with 3-state outputs**. It delivers high resiliency to single-event effects (SEE) and to a total ionizing dose (TID) to 30 krad (Si). This device is a member of the Apogee Semiconductor AP54RHC logic family. It operates across a 1.4 V to 5.5 V range on both of its supply voltage inputs, $V_{CC}A$ and $V_{CC}Y$.

Zero-power penalty™ cold sparing is supported. A proprietary output stage and robust power-on reset (POR) circuit allow the AP54RHC804 to be cold-spared in any redundant configuration with no static power loss. The redundant output stage also features a high drive capability with low static power loss.

Ordering information may be found in Table 10 on Page 15. A Geosynchronous Earth Orbit (GEO) variant with 300 krad (Si) TID assurance is also available in the AF54RHC804.

1.1 DEVICE INFORMATION

PART NUMBER	GRADE	Package
AP54RHC804ANT(1)	A-Grade Flight (LEO)	TSSOP-20 Plastic mass 74 mg
AP54RHC804BNT(1)	B-Grade Flight (LEO)	
AP54RHC804CNT(1)	C-Grade Flight (LEO)	
AP54RHC804ENT	E-Grade (Evaluation)	

(1) Release in June 2026.

1.2 APPLICATIONS

- Voltage level translation
- LVCMOS FPGA I/O level translation
- Telemetry data interfacing
- Multi-voltage system level interfacing
- Sensor integration
- Bi-directional level shifting

1.3 FEATURES

- SEL immune to LET of 75 MeV-cm^2/mg
- 1.4 V to 5.5 V operation
- Inputs tolerant up to 5.5 V at any $V_{CC}A$
- Provides logic-level translation to $V_{CC}Y$
- Cold sparing Inputs and Outputs
- TID RLAT 30 krad (Si) at 5.5 V
- Operating temperature range -55 °C to +125 °C
- Meets NASA's ASTM E595 outgassing specification
- Moisture sensitivity level 1 (unlimited)

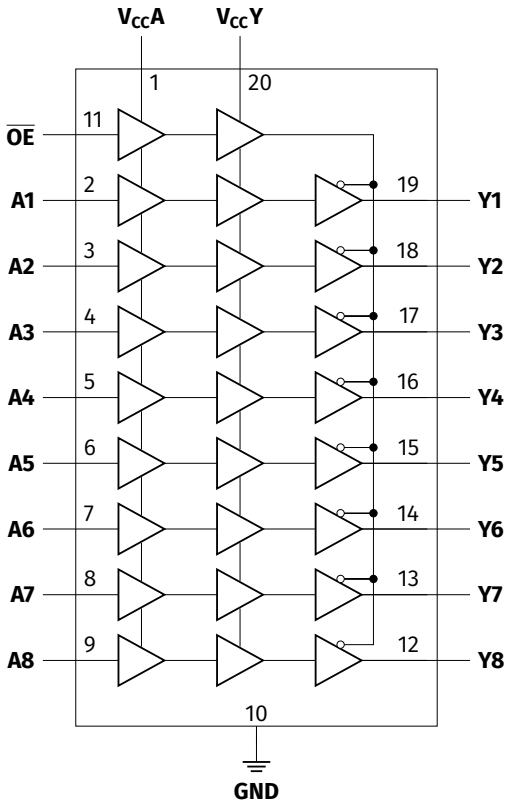

Figure 1: AP54RHC804 Logic Diagram

† See detailed note.

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2 ACRONYMS AND ABBREVIATIONS

ESD	Electrostatic Discharge
POR	Power On Reset
RHA	Radiation Hardness Assurance
SEE	Single Event Effects
SEL	Single Event Latchup
SET	Single Event Transient
TID	Total Ionizing Dose
TMR	Triple Modular Redundancy
CDM	Charged-device Model
HBM	Human-body Model

3 LOGIC DATA

The AP54RHC804 truth table is found in Table 1. **H** indicates HIGH logic level, **L** indicates LOW logic level, **X** indicates DON'T CARE and **Z** indicates HIGH-Z (TRI-STATE). Subscript **n** reflects one of the eight buffers in the device (1 to 8).

Table 1: AP54RHC804 Device Truth Table

Inputs		Output
$\overline{OE}$	A_n	Y_n
L	L	L
L	H	H
H	X	Z

4 PIN CONFIGURATION

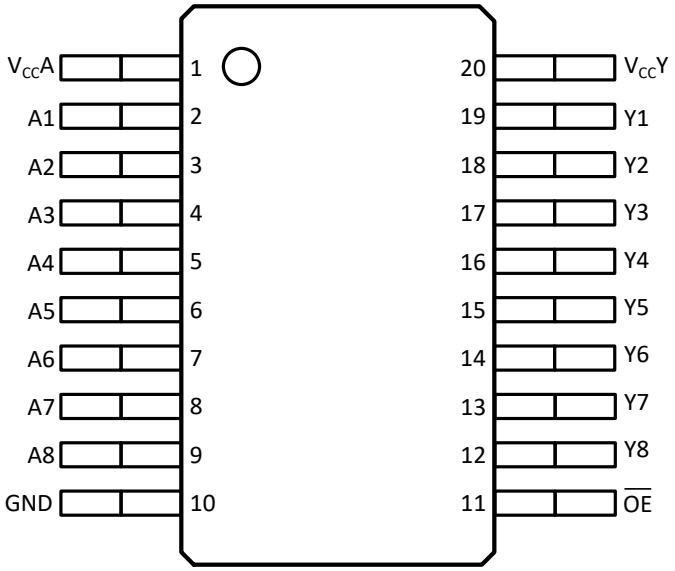


Figure 2: AP54RHC804 Device Pinout

Table 2: AP54RHC804 Device Pinout

PIN NAME(S)	PIN NUMBER(S)	DESCRIPTION
A1 A2 A3 A4 A5 A6 A7 A8	2 3 4 5 6 7 8 9	Signal Inputs. Referenced to $V_{CC}A$.
Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8	19 18 17 16 15 14 13 12	Signal Outputs. Referenced to $V_{CC}Y$.
$\overline{OE}$	11	Output Enable (active-low). Referenced to $V_{CC}A$.
$V_{CC}A$	1	Positive Voltage Supply (A Side)
$V_{CC}Y$	20	Positive Voltage Supply (Y Side)
GND	10	Ground

5 ELECTRICAL CHARACTERISTICS

The sign convention for current follows JEDEC standards with negative values representing current sourced from the device and positive values representing current sunk into the device. All parameters in this section are specified across the entire operating temperature range unless otherwise specified. For A-grade flight and B-grade flight parts, all parameters are specified over the entire recommended voltage range of 1.4 V to 5.5 V. For C-grade flight and E-grade Evaluation parts, all parameters are specified over the voltage range of 1.65 V to 5.5 V.

5.1 ABSOLUTE MAXIMUM RATINGS

Excursions beyond the values listed in Table 3 may cause permanent damage to the device. Proper function of the device cannot be guaranteed if these values are exceeded, and long-term device reliability may be affected. Functionality of the device at these values, or beyond those listed in Recommended Operating Conditions (Table 4) is not guaranteed.

Table 3: Absolute Maximum Ratings

SYMBOL	PARAMETER		VALUE	UNITS
$V_{CC}A$, $V_{CC}Y$	Supply Voltage		-0.5 to +5.5	V
V_I	Input voltage range		-0.5 to +5.5	V
V_O	Output voltage range		-0.5 to + 5.5	V
I_{IK} (V_I < 0)	Input clamp current		100	mA
I_O	Continuous output current (per pin)		100	mA
I_{CC}	Maximum supply current		100	mA
V_{ESD}	ESD Voltage	HBM	1000	V
		CDM	500	V
T_J	Operating junction temperature range		-55 to +150	°C
T_{STG}	Storage temperature range		-65 to +150	°C

5.2 RECOMMENDED OPERATING CONDITIONS

Table 4: Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	MAX	UNITS
$V_{CC}A$, $V_{CC}Y$	Supply voltage (A-grade flight, B-grade flight)		1.4	5.5	V
$V_{CC}A$, $V_{CC}Y$	Supply voltage (C-grade flight, E-grade Evaluation)		1.65	5.5	V
V_I	Input voltage range		0	5.5	V
V_O	Output voltage range		0	$V_{CC}Y$	V
V_{IH}	HIGH-level input voltage	$V_{CC}A$ = 1.4 to 1.6 V	1.12	-	V
		$V_{CC}A$ = 1.65 to 1.95 V	1.4	-	
		$V_{CC}A$ = 2.3 to 2.7 V	1.9	-	
		$V_{CC}A$ = 3.0 to 3.6 V	2.5	-	
		$V_{CC}A$ = 4.5 to 5.5 V	3.8	-	
V_{IL}	LOW-level input voltage	$V_{CC}A$ = 1.4 to 1.6 V	-	0.32	V
		$V_{CC}A$ = 1.65 to 1.95 V	-	0.4	
		$V_{CC}A$ = 2.3 to 2.7 V	-	0.6	
		$V_{CC}A$ = 3.0 to 3.6 V	-	0.9	
		$V_{CC}A$ = 4.5 to 5.5 V	-	1.35	
I_{OH}	HIGH-level output current	$V_{CC}Y$ = 1.4 to 1.6 V	-	-2	mA
		$V_{CC}Y$ = 1.65 to 1.95 V	-	-4	
		$V_{CC}Y$ = 2.3 to 2.7 V	-	-8	
		$V_{CC}Y$ = 3.0 to 3.6 V	-	-16	
		$V_{CC}Y$ = 4.5 to 5.5 V	-	-24	
I_{OL}	LOW-level output current	$V_{CC}Y$ = 1.4 to 1.6 V	-	2	mA
		$V_{CC}Y$ = 1.65 to 1.95 V	-	4	
		$V_{CC}Y$ = 2.3 to 2.7 V	-	8	
		$V_{CC}Y$ = 3.0 to 3.6 V	-	16	
		$V_{CC}Y$ = 4.5 to 5.5 V	-	24	
t_r, t_f	Input rise or fall time (10% - 90%)	$V_{CC}A$ = 1.4 to 1.6 V	-	2000	ns
		$V_{CC}A$ = 1.65 to 1.95 V	-	1000	
		$V_{CC}A$ = 2.3 to 2.7 V	-	600	
		$V_{CC}A$ = 3.0 to 3.6 V	-	500	
		$V_{CC}A$ = 4.5 to 5.5 V	-	400	

Table 5: Thermal Information

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
T_J	Operating junction temperature	-55	-	+125	°C
$R_{\theta JA}$	Junction to ambient thermal resistance	-	100	-	°C/W

5.3 STATIC CHARACTERISTICS

Table 6: DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	V_{CC}	MIN	TYP	MAX	UNITS
V_{OL}	LOW-Level Output Voltage[1]	I_O = 100 µA	1.4 to 5.5 V	-	0.02	0.05	V
		I_O = 1 mA	1.4 to 5.5 V	-	0.05	0.15	V
		I_O = 2 mA	1.4 V	-	0.18	0.4	V
		I_O = 4 mA	1.65 V	-	0.27	0.8	V
			2.3 V	-	0.3	0.6	V
			3.0 V	-	0.2	0.4	V
			4.5 V	-	0.2	0.4	V
		I_O = 8 mA	2.3 V	-	0.6	1.0	V
			3.0 V	-	0.4	0.8	V
			4.5 V	-	0.3	0.6	V
		I_O = 16 mA	3.0 V	-	1.0	1.4	V
			4.5 V	-	1.1	1.2	V
		I_O = 24 mA	4.5 V	-	1.1	1.5	V
V_{OH}	HIGH-Level Output Voltage[1]	I_O = -100 µA	1.4 to 5.5 V	$V_{CC}Y$ - 0.1	$V_{CC}Y$ - 0.02	-	V
		I_O = -1 mA	1.4 to 5.5 V	$V_{CC}Y$ - 0.15	$V_{CC}Y$ - 0.08	-	V
		I_O = -2 mA	1.4 V	0.9	1.2	-	V
		I_O = -4 mA	1.65 V	1	1.35	-	V
			2.3 V	1.8	2.0	-	V
			3.0 V	2.6	2.7	-	V
			4.5 V	4.2	4.4	-	V
		I_O = -8 mA	2.3 V	1.4	1.7	-	V
			3.0 V	2.2	2.5	-	V
			4.5 V	3.9	4.1	-	V
		I_O = -16 mA	3.0 V	1.5	2.0	-	V
			4.5 V	3.3	3.8	-	V
		I_O = -24 mA	4.5 V	3.0	3.5	-	V
$I_{CC}Y$	Quiescent supply current	V_I = $V_{CC}A$ or GND $\overline{OE}$ = GND I_O = 0 mA	1.6 V	-	35	55	µA
			1.95 V	-	45	70	µA
			3.6 V	-	115	150	µA
			5.5 V	-	215	250	µA
		Same as above; T_a = 25°C Post TID	1.6 V	-	170	190	µA
			1.95 V	-	180	210	µA
			3.6 V	-	250	285	µA
			5.5 V	-	350	385	µA
I_I	Input current	V_I = $V_{CC}A$ or GND	1.4 to 5.5 V	-1	-	1	µA
I_{OZ}	Output leakage current[2]	V_I = $V_{CC}Y$ or GND $\overline{OE}$ = $V_{CC}A$	1.4 to 5.5 V	-	-	±2.5	µA
I_{OFF}	Pwrdwn leakage current[2, 3]	V_I = GND to 5.5 V	OFF	-	-	5	µA
$I_{CC}A$	Quiescent supply current	V_I = $V_{CC}A$ or GND I_O = 0 mA	1.6 V	-	9	25	µA
			1.8 V	-	10	35	µA
			3.5 V	-	20	60	µA
			5.5 V	-	30	100	µA

[1] $V_{CC}A$ = 1.4 to 5.5 V for these conditions [2] $V_{CC}Y$ = 0 to 5.5 V for these conditions [3] $V_{CC}A$ is at GND potential

5.4 DYNAMIC CHARACTERISTICS

Table 7: AC Electrical Characteristics. C_L = 50 pF

Symbol	Parameter	$V_{CC}A$	$V_{CC}Y$ 1.5 ±0.1 V		$V_{CC}Y$ 1.8 ±0.15 V		$V_{CC}Y$ 2.5 ±0.2 V		$V_{CC}Y$ 3.3 ±0.3 V		$V_{CC}Y$ 5 ±0.5 V		Units
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
t_{pd}	Propagation Delay (Input **A** to Output **Y**)	1.5 ±0.1 V	24.5	60	15.6	41	10.6	23	8.9	20	8.2	18	ns
		1.8 ±0.15 V	18.5	60	11.8	25	7.9	15	6.2	13	5.8	11	ns
		2.5 ±0.2 V	18	60	11.3	25	7.4	15	5.6	13	4.3	11	ns
		3.3 ±0.3 V	17.8	60	11.2	25	7.2	15	5.4	13	4.2	11	ns
		5 ±0.5 V	17.7	60	11.1	25	7.1	15	5.3	13	3.9	11	ns
t_{dis}	Output Disable Time (Input $\overline{\textbf{OE}}$ to Output **Y**)	1.5 ±0.1 V	30.1	45	25.9	40	22.6	37	21.8	35	21.8	33	ns
		1.8 ±0.15 V	27.3	80	18.3	53	17.2	41	17.1	35	18.2	25	ns
		2.5 ±0.2 V	26.8	80	17.9	53	16.7	41	16.3	35	16.2	25	ns
		3.3 ±0.3 V	26.1	80	17.7	53	16.6	41	16.1	35	15.9	25	ns
		5 ±0.5 V	26	80	17.7	53	16.5	41	16.1	35	15.9	25	ns
t_{en}	Output Enable Time (Input $\overline{\textbf{OE}}$ to Output **Y**)	1.5 ±0.1 V	56.5	91	38.6	69	24.4	42	20.9	36	19.3	31	ns
		1.8 ±0.15 V	47	80	21.7	53	17.3	41	15.5	35	15.1	25	ns
		2.5 ±0.2 V	46.5	80	21.4	53	16.9	41	15.0	35	13.7	25	ns
		3.3 ±0.3 V	46.3	80	21.3	53	16.8	41	14.9	35	13.5	25	ns
		5 ±0.5 V	46.4	80	21.4	53	17.0	41	15.0	35	13.6	25	ns

Table 8: AC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	$V_{CC}Y$	MIN	TYP	MAX	UNITS
t_{sk}	Channel-to-channel skew[(1)]	C_L = 50 pF	1.4 to 5.5 V	-	-	1	ns
C_{in}	Input Capacitance[(1)]	V_I = V_{CC} or GND	1.4 to 5.5 V	-	2	4	pF
C_{pd}	Power Dissipation Capacitance[(1)]	I_O = 0 mA, f = 1 MHz	5.5 V	-	40	-	pF

(1) guaranteed by design

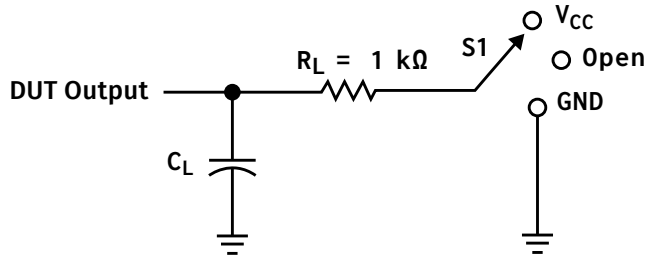
5.5 RADIATION RESILIENCE

For detailed radiation testing reports, please contact Apogee Semiconductor at sales@apogeesemi.com.

Table 9: Radiation Resilience Characteristics

PARAMETER	CONDITIONS	VALUE	UNITS
Total Ionizing Dose (TID)	Please contact Apogee Semiconductor for test report.	30	krad (Si)
SEL Onset LET Threshold	Please contact Apogee Semiconductor for test report.	≥75	MeV-cm^2/mg

5.6 CHARACTERISTICS MEASUREMENT INFORMATION



TEST	S1
t_{pd}	GND
t_{PLZ}, t_{PZL}	V_{CC}
t_{PHZ}, t_{PZH}	GND

Figure 3: Load Circuit for 3-State Outputs

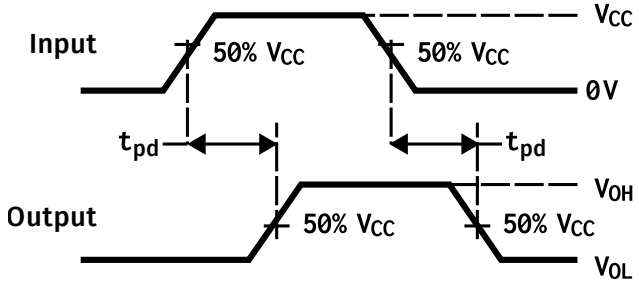


Figure 4: Propagation Delay Measurement

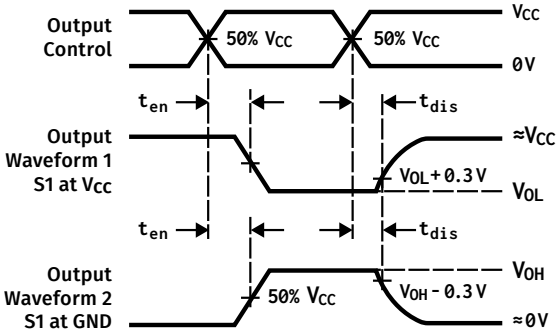


Figure 5: Enable and Disable Time Measurements

6 DETAILED DESCRIPTION

The AP54RHC804 is a 8-channel level translator with 3-state outputs designed to operate from a wide supply voltage of 1.4 to 5.5 V with fully redundant input and output stages, providing for superior radiation resilience.

The output and input stages are constructed with transient-activated clamps (Figure 6, Figure 7) that prevent inadvertent biasing of the V_{CC} power rail through parasitic diodes inherent to conventional input, output, and ESD circuits. The IC also incorporates an internal power-on reset (POR) circuit guaranteeing correct operation at power supply voltages as low as 1.4V.

The AP54RHC family's I/O protection circuitry allows for cold sparing configurations as it avoids a leakage current penalty on inputs and outputs while in a power-down state. This can result in considerable power savings in systems where multiple-path redundancy is employed. The ESD clamp circuits for this logic family are designed to support Class 1C ESD levels of 1 kV HBM and 500 V CDM.

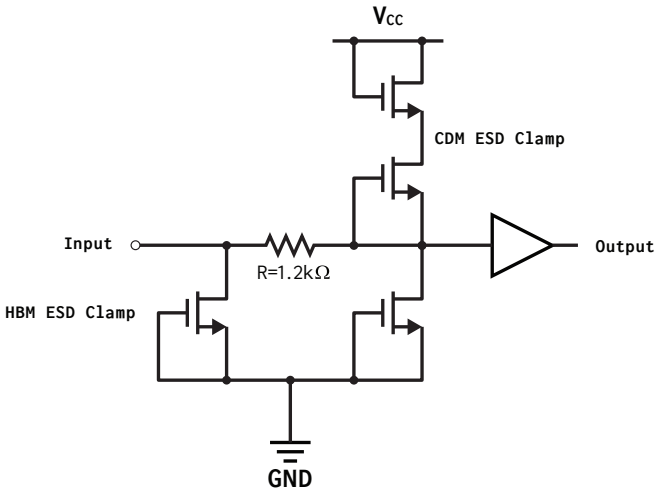


Figure 6: Input Pin Structure

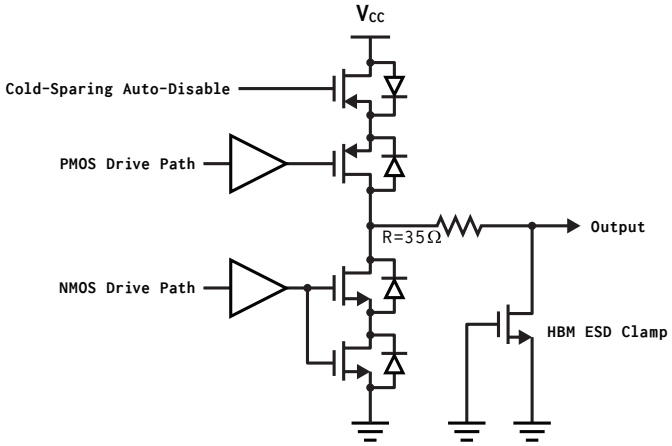


Figure 7: Output Pin Structure

7 APPLICATIONS INFORMATION

The AP54RHC804 provides a simple and robust means of interfacing digital logic between different voltage levels and domains. It can shift logic signals up from a lower voltage to a higher voltage or shift signals down from higher to lower voltages.

It offers several features that make interfacing between different domains simple. First, the absence of an input supply voltage results in a tri-state condition at the output. Second, the outputs may also be tri-stated through assertion of the $\overline{OE}$ pin, which can be tied with power-supply enables or other control signals.

In an application utilizing a modern FPGA with 1.5 V I/O buffers that needs to interface to systems running at higher voltages (i.e. 5 V), the AP54RHC804 can be used to shift these signals to a range appropriate for the FPGA. The AP54RHC804 provides integrated triple modular redundancy (TMR), as well as SET resiliency on each buffer. In the event the 5 V supply is off, the AP54RHC804 will automaticaly tri-state the output buffers. The $\overline{OE}$ pin of the device can be tied to the FPGA power-enable logic such that $\overline{OE}$ is de-asserted when the 1.5 V I/O rail is not present. Figure 8 shows an example of a Versal FPGA utilizing two AP54RHC804 and an AP54RHC301 majority voter to add additional redundancy for critical control and telemetry signals with error feedback. See the AP54RHC301 product folder

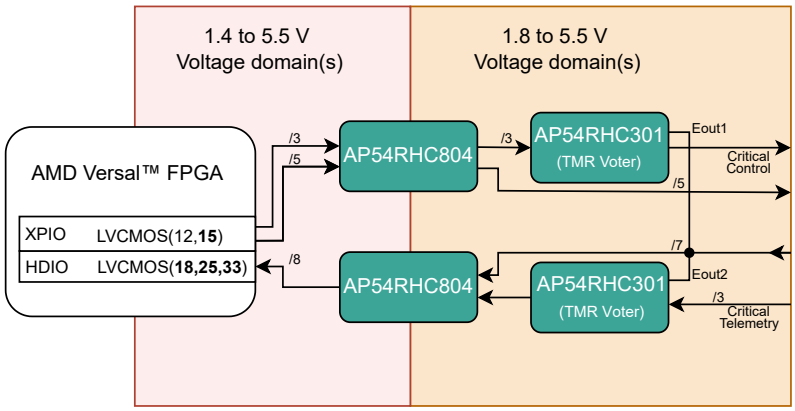


Figure 8: Level Shifting utilizing AP54RHC804

Figure 9 shows a multi-domain level shifting application using AP54RHC804 and an APIO16 radiation hardened I/O expander. In this configuration, the APIO16 is used to level shift to and from the low voltage 1.5 V domain to the 3.3 V domain. The AP54RHC804s are used to level shift to and from the 3.3 V domain to the 5 V domain. The APIO16 provides 16 additional input or output channels that can be used to expand the I/O capabilities of a processor or FPGA with limited I/O resources. It can be controlled via a simple I^2C or SPI interface. See the APIO16 product folder for more information.

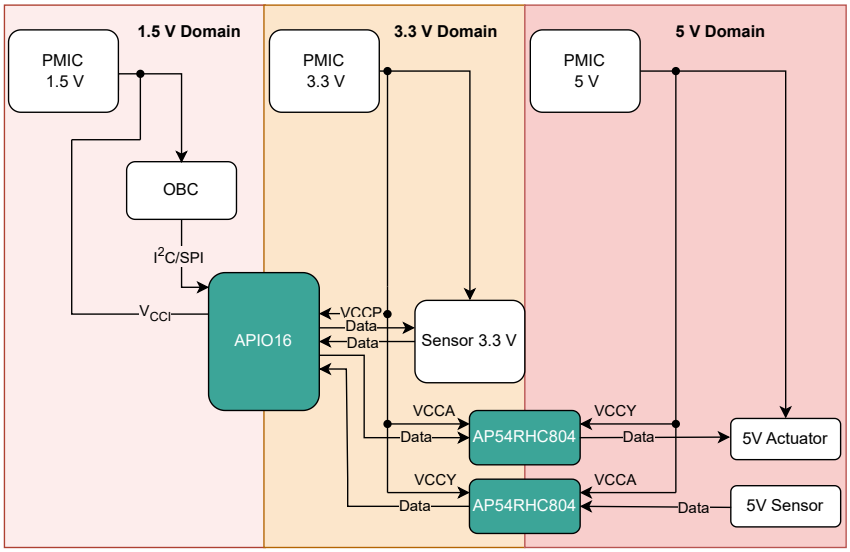


Figure 9: Multi DomainLevel Shifting using AP54RHC804 and APIO16

Two AP54RHC804 devices can be used in conjunction to create a bi-directional level shifter. In this application, the $\overline{OE}$ signal of one of the level shifters is driven by a control signal, and the $\overline{OE}$ of the second level shifter is driven by an inverted version of this signal, so that only one device is enabled at a time. The outputs of the non-enabled device will be tri-stated, enabling the same PCB lines to be used to connect both sides of the bi-directional level shifter. The $\overline{OE}$ signal is referenced to the higher voltage domain since it is acceptable to overdrive the $\overline{OE}$ signal to the lower voltage domain device.

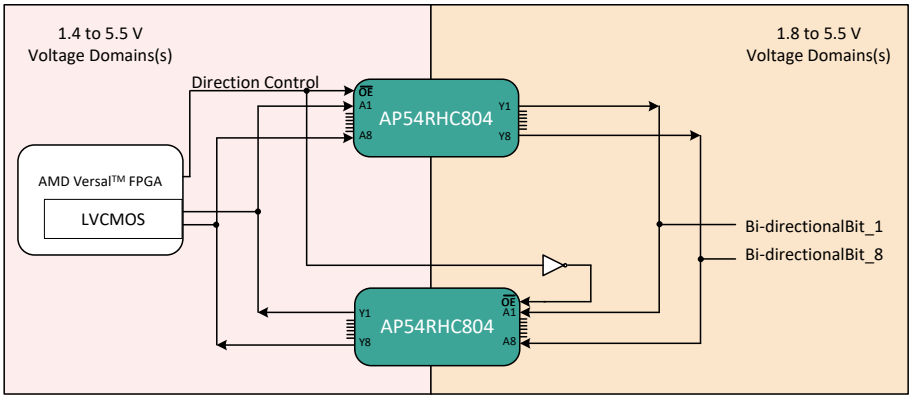


Figure 10: Bi-directional Level Shifting using Two AP54RHC804 Devices

7.1 USE IN COLD-SPARING CONFIGURATIONS

As the AP54RHC family is radiation-hardened by design and includes internal TMR, it can be utilized in high-reliablity applications without additional supporting circuitry or devices. Nonetheless, some application requirements call for fully-redundant designs, where an “A” and a “B” device are required, often on separate power rails.

With the cold sparing capability of the AP54RHC family, fully redundant “A” and “B” functions may be placed in parallel (Figure 11) running off redundant power supplies. The inputs and outputs on each one of these functions are assumed to be based on the AP54RHC family, allowing for direct parallel connection without unwanted leakage current paths during cold sparing. In the event of a failure in power supply A or within function A,

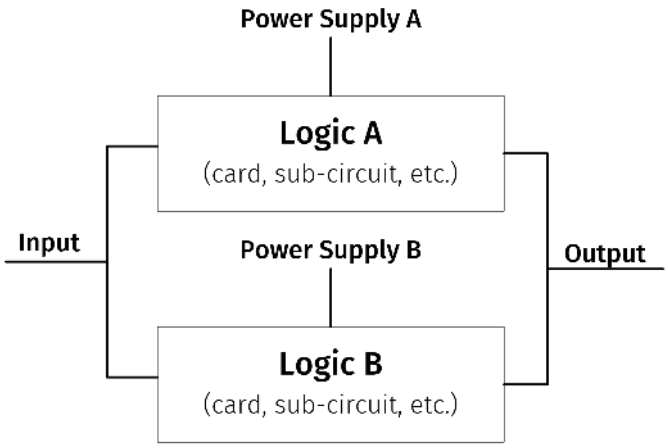


Figure 11: Two-Path Cold-Sparing Configuration

the system can simply shut power supply A off and switch on power supply B, without requiring additional input or output switching or configuration changes.

7.2 POWER SUPPLY RECOMMENDATIONS

This device can operate at any voltage within the range specified in Table 4 Recommended Operating Conditions.

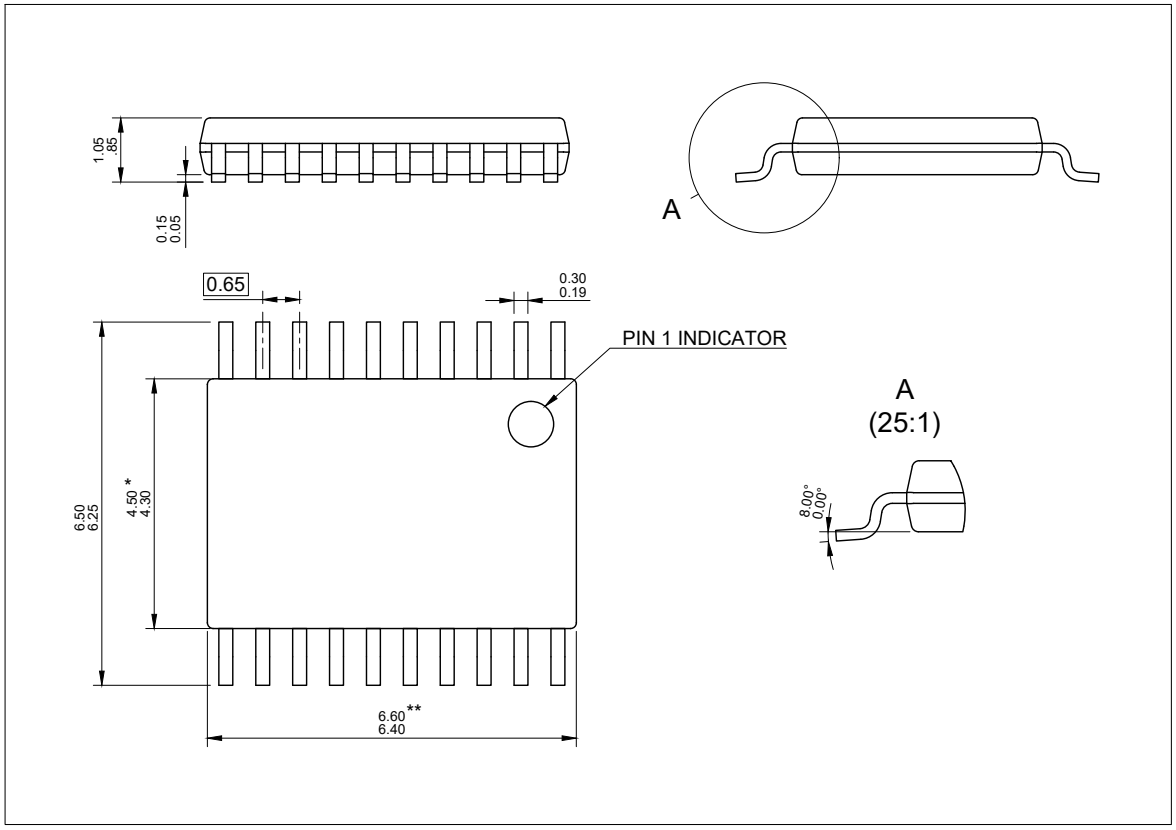
At a minimum, a 16 VDC (or higher), X7R-rated 0.1 µF ceramic decoupling capacitor should be placed near (within 1 cm) the V_{CC} pins of the device.

7.3 APPLICATION TIPS

Unused **inputs** must **not** be left floating. They may be connected to either a low (GND) or high (V_{CC}A) bias to provide a known state at the input of the device. Resistors may be used to tie off unused inputs. In the event of a design change, such resistors can be removed, thereby allowing use of the inputs without having to cut traces on the PCB.

An unused **output** may be left unconnected. However, if the output is held in tristate, it is recommended to weakly bias the output to a valid logic level to prevent increased supply current. It is suggested that it be routed to a test point or similar accessible structure in case the associated function needs to be utilized as part of a design revision.

8 PACKAGING INFORMATION



Notes:
1. All linear dimensions are in millimeters. Dimensioning and tolerancing are as per ISO/TS 128-71:2010
2. The part is compliant with JEDEC MO-153 specifications.

* Body width does **not** include interlead flash. Interlead flash shall not exceed 0.25 mm each side.
** Body length does **not** include mold flash, protrusion, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0.15 mm on each side.

Figure 12: Package Mechanical Drawing

9 ORDERING INFORMATION

Example part numbers for the AP54RHC804 are listed in Table 10. The full list of options for this part can be found in Figure 13. For a detailed description of product grades, please refer to Product Grades and Quality Flows document. Please contact Apogee Semiconductor sales at sales@apogeesemi.com for further information on sampling, lead time and purchasing on specific part numbers.

Table 10: AP54RHC804 Ordering Information

DEVICE	DESCRIPTION	PACK-AGING	PACKAGE	LEAD FINISH	STATUS
AP54RHC804ANT-R	Rad-Hard 8-Channel Level Translator, A-Grade Flight (LEO)	Reel	TSSOP-20	NiPdAu	Plan Rls JUN-2026
AP54RHC804BNT-R	Rad-Hard 8-Channel Level Translator, B-Grade Flight (LEO)	Reel	TSSOP-20	NiPdAu	Plan Rls JUN-2026
AP54RHC804CNT-R	Rad-Hard 8-Channel Level Translator, C-Grade Flight (LEO)	Reel	TSSOP-20	NiPdAu	Plan Rls JUN-2026
AP54RHC804ENT-R	8-Channel Level Translator E-Grade (for evalulation only)	Reel	TSSOP-20	NiPdAu	Available

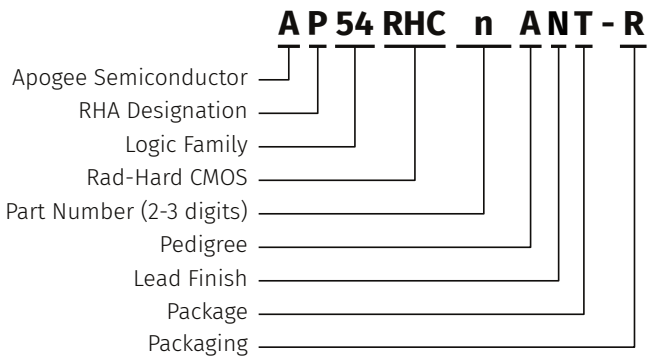


Figure 13: Part Number Decoder

1. RHA Designation
   - **P** 30 krad (Si)
   - **F** 300 krad (Si)
2. Part Number
   - **_** 804 (8-Channel Level Translator)
3. Pedigree
   - **A** -55 to +125 °C (Burn-in)
   - **B** -55 to +125 °C (No burn-in)
   - **C** 25 °C (No burn-in)
   - **E** 25 °C Functional Test Only (Evaluation)
4. Lead Finish
   - **N** Nickel-Palladium-Gold (NiPdAu)
5. Package
   - **T** 20-pin Thin Shrink Small Outline Package (TSSOP)
6. Packaging
   - **R** Tape and Reel[(1)]

[(1)] Contact us for custom reel quantities. Orders less than full reel quantities may be shipped as cut tape.

10 REVISION HISTORY

REVISION	DESCRIPTION	DATE
B00	Initial release	2026-May-06

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11 LEGAL

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