ARPS1020A5 / ARPS1050A5

Radiation–Hardened 50 V, 4 A / 20 V, 8 A Smart High–Side Power Switch Family

1 GENERAL DESCRIPTION

The **ARPS1020A5 / ARPS1050A5** is a radiation-hardened by design family of power switches with integrated FET that is ideally suited for space, and other applications demanding radiation tolerance and high reliability. The family delivers high resiliency to total ionizing dose (TID) and single-event effects (SEE).

The 50 V variant supports the 28 V nominal bus voltage typically found in power distribution systems of a spacecraft, while the 20 V variant is ideal for a 12 V bus or at lower voltage loads such as 5 V and 3 V. With a 3 mm × 5 mm space-grade plastic package, the switch can also benefit compact phased array systems where power switching of amplifier elements is needed. The devices offer a user-configurable current trip threshold as well as a current sense telemetry output. Higher current applications are enabled by multiple switches in parallel.

1.1 DEVICE INFORMATION

PART NUMBER	GRADE	Package
ARPS1020A5ANQ	A-Grade Flight[1] (LEO/GEO)	QFN-24 Plastic 3 × 5 mm mass = 39.7 mg
ARPS1050A5ANQ		
ARPS1020A5BNQ	B-Grade Flight[1] (LEO/GEO)	
ARPS1050A5BNQ		
ARPS1020A5CNQ	C-Grade Flight[1] (LEO/GEO)	
ARPS1050A5CNQ		
ARPS1020A5ENQ	E-Grade	
ARPS1050A5ENQ		
ARPS10x0-x-EVB	E-Grade EVB (Eval Board)	EVB

[1] Planned release JUN-2026

1.2 APPLICATIONS

- Power distribution systems
- Load shedding
- Switching of cold spared power domains
- Heater switching
- Load current monitoring for on-orbit bias tuning
- Load current monitoring for latchup detection
- Fine granularity power domain latchup recovery

1.3 FEATURES

- 3 V to 50 V / 3 V to 20 V DC operation
- 20 V, 8 A, 23 mΩ RDSon / 50 V, 4 A, 57 mΩ RDSon
- 3 mm × 5 mm QFN with ePAD
- True current sharing supports parallel configuration for higher current/lower RDSon applications
- Configurable soft-start ramp speed and overcurrent protection
- Current sense output for external telemetry
- Built in over-temperature protection and power up into short-circuit protection
- OFF output pin indicates when switch is fully disabled. Enables active discharge or break-before-make switching
- TID resilience: 100 krad (Si)
- SEB/SEGR immune at LET of 73 MeV-cm^2/mg: VIN = 20 V (ARPS1020A5), VIN = 36 V (ARPS1050A5)
- SEFI/SET resilience: Radiation Report to be published
- Moisture sensitivity level: MSL 1

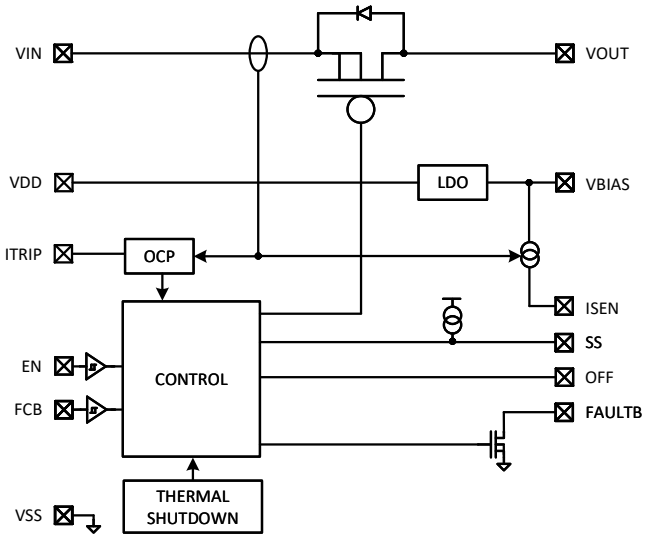

Figure 1: Block Diagram of Monolithic IC

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2 ACRONYMS AND ABBREVIATIONS

ESD	Electrostatic Discharge
RHA	Radiation Hardness Assurance
SEFI	Single Event Functional Interrupt
SET	Single Event Transient
TMR	Triple Modular Redundancy
HBM	Human-body Model
POR	Power On Reset
SEE	Single Event Effects
SEL	Single Event Latchup
TID	Total Ionizing Dose
CDM	Charged-device Model

3 PIN CONFIGURATION

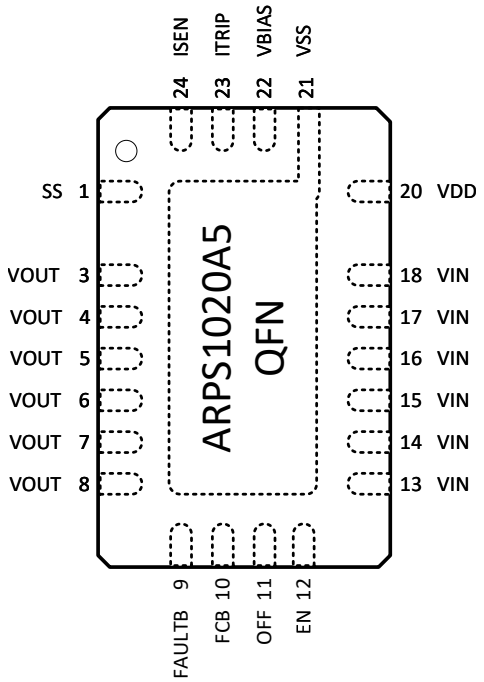

Figure 2: ARPS1020A5 Device Pinout (Top View)

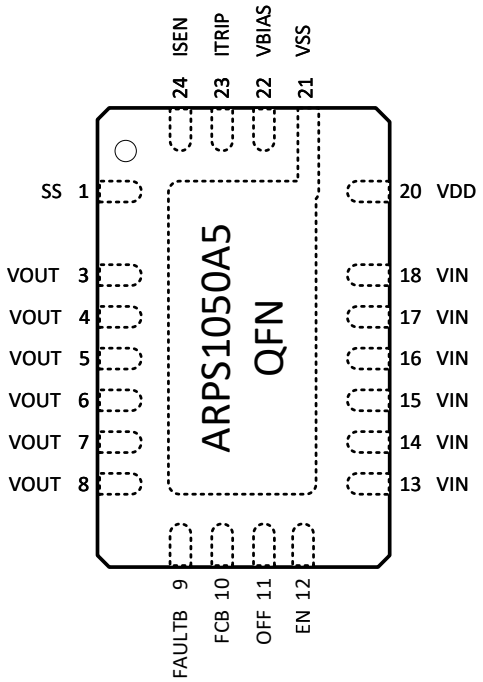

Figure 3: ARPS1050A5 Device Pinout (Top View)

Table 1: ARPS1020A5 / ARPS1050A5 Device Pinout Description

PIN NAME(S)	PIN NUMBER(S)	DESCRIPTION
ITRIP	23	Resistor to ground sets overcurrent trip level
ISEN	24	Current sense output for telemetry
SS	1	Capacitor to VSS, sets softstart time
VOUT	3, 4, 5, 6, 7, 8	Switched output
FAULTB	9	Open drain output indicating a fault has occurred
EN	12	Active high input to enable the power switch
OFF	11	Active high indicates when power switch is disabled
FCB	10	Active low input to clear faults, must set high to enable power switch
VIN	13, 14, 15, 16, 17, 18	Switched input
VDD	20	Input supply for internal LDO and circuitry
VSS	21, ePAD	Ground
VBIAS	22	Internal LDO output, connect a nominal 220 nF ceramic capacitor to ground

4 ELECTRICAL CHARACTERISTICS

The sign convention for current follows JEDEC standards with negative values representing current sourced from the device and positive values representing current sunk into the device.

4.1 ABSOLUTE MAXIMUM RATINGS

Excursions beyond the values listed in Table 2 may cause permanent damage to the device. Proper function of the device cannot be guaranteed if these values are exceeded, and long-term device reliability may be affected. Functionality of the device at these values, or beyond those listed in Recommended Operating Conditions (see Table 3) is not guaranteed.

All parameters are specified across the entire operating temperature range unless otherwise specified.

Table 2: Absolute Maximum Ratings

SYMBOL	PARAMETER		VALUE	UNITS
VOUT	Output Voltage	ARPS1050A5	-1 to +55	V
		ARPS1020A5	-1 to +22	V
V_{DD}, VIN	Supply Voltage	ARPS1050A5	-0.3 to +55	V
		ARPS1020A5	-0.3 to +22	V
V_{BIAS}	VBIAS		-0.3 to +2.0	V
ITRIP, ISEN, SS, OFF	I/O Pin Voltage		-0.3 to VBIAS +0.3	V
EN, FCB, FAULTB	I/O Pin Voltage		-0.3 to 5.5	V
V_{ESD}	ESD Voltage	HBM	> 500	V
		CDM	> 500	V
T_J	Operating junction temperature range		-55 to +150	°C
T_{STG}	Storage temperature range		-65 to +150	°C

4.2 RECOMMENDED OPERATING CONDITIONS

All recommended parameters below are specified across the entire operating temperature range unless otherwise specified.

Table 3: Recommended Operating Conditions

(Refer to radiation report for SEE limits.)

SYMBOL	PARAMETER		MIN	MAX	UNITS
VIN	Voltage on VIN pin or VOUT pin (Disabled)	ARPS1050A5	0	50	V
		ARPS1020A5	0	20	
	Voltage on VIN pin or VOUT pin (Enabled)	ARPS1050A5	3	50	
		ARPS1020A5	3	20	
V_{DD}	Supply voltage	ARPS1050A5	3	50	V
		ARPS1020A5	3	20	
SR_{VIN}	Voltage slew rate on VIN pin			0.4	V/us
SR_{VDD}	Voltage slew rate on VDD pin			0.4	V/us
I_{MAX}	Maximum continuous switch current	ARPS1050A5	-	4	A
		ARPS1020A5	-	8	

Table 4: Thermal Information

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
T_J	Operating junction temperature	-55	-	+125	°C
$R_{\theta JC\_BOT}$	Junction to case (bottom) thermal resistance	-	1.5 TBD	-	°C/W

4.3 ELECTRICAL CHARACTERISTICS

All parameters are specified across the entire operating temperature range unless otherwise specified.

Table 5: Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD_START}	V_{DD} UVLO start voltage		2.1	2.55	2.95	V
V_{DD_STOP}	V_{DD} UVLO stop voltage		2.0	2.39	2.85	V
V_{DD_HYST}	V_{DD} UVLO hysteresis		0.10	0.16	-	V
V_{IN_START}	V_{IN} UVLO start voltage		2.4	2.6	2.9	V
V_{IN_STOP}	V_{IN} UVLO stop voltage		2.3	2.51	2.8	V
V_{IN_HYST}	V_{IN} UVLO hysteresis		0.05	0.09	-	V
V_{T+}	EN/FCB Positive-going threshold voltage		0.58	0.74	0.91	V
V_{T-}	EN/FCB Negative-going threshold voltage		0.56	0.7	0.89	V
ΔV_T	EN/FCB Input hysteresis (V_{T+}-V_{T-})		0.02	0.04	-	V
V_{OH_OFF}	OFF pin high level output voltage	I_{OFF} = -100 uA	1.5	1.8	1.9	V
V_{OL_OFF}	OFF pin low level output voltage	I_{OFF} = +2 mA	-	80	150	mV
I_{LK_OFF}	OFF pin off-state leakage	V_{OFF} = 2 V, VBIAS = 0 V, VDD = 0 V	-	-	5	uA
V_{OL_FAULTB}	FAULTB pin low level output voltage	I_{FAULTB} = + 2 mA	-	25	50	mV
I_{LK_FAULTB}	FAULTB pin off-state leakage	V_{FAULTB} = 5.5 V	-	-	5	uA
I_{EN}	Pull up current sourced from EN pin	V_{EN} = 1 V	1	3.96	6	uA
I_{FAST}(1)	Fast current protection trip level		I_{MAX} × 1.2	I_{MAX} × 2	-	A
t_{IFAST}(1)	Fast current protection time		-	15	-	us
K_{ISLOW}	Islow trip gain	ARPS1050A5	-10%	40000	+10%	A/A
		ARPS1020A5	-10%	80000	+10%	
t_{ISLOW}	Slow current protection time		11.0	12.25	13.5	ms
I_{SS}	Current sourced out of SS pin during softstart		9	10	11	uA

Table 5: Electrical Characteristics (continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{SOFT-START\_T}$	Voltage on SS pin at which power switch turns fully on		0.95	1.0	1.1	V
K_{SS}	Soft-start gain	ARPS1050A5, $V_{SOFT-START}$ = 0.4 V	TBD	5.0	TBD	A/V
		ARPS1020A5, $V_{SOFT-START}$ = 0.4 V	TBD	10	TBD	
K_{ISENSE}	I-Sense gain	ARPS1050A5, I_{OUT} = 1 A	-6%	4000	+6%	A/A
		ARPS1020A5, I_{OUT} = 2 A	-6%	8000	+6%	
R_{ON}	ON resistance VIN to VOUT	ARPS1050A5, I_{OUT} = 200 mA	-	57	94	mΩ
		ARPS1020A5, I_{OUT} = 200 mA	-	23	34	
I_{OFF}	Off-state leakage current (VIN to VOUT) for ARPS1050A5	V_{IN} = VIN MAX, V_{OUT} = 0 V, V_{EN} = 0 V, V_{FCB} = 0 V, T_J=25°C	-	5	100	uA
		V_{IN} = VIN MAX, V_{OUT} = 0 V, V_{EN} = 0 V, V_{FCB} = 0 V, T_J=125°C	-	50	500	
	Off-state leakage current (VIN to VOUT) for ARPS1020A5	V_{IN} = VIN MAX, V_{OUT} = 0 V, V_{EN} = 0 V, V_{FCB} = 0 V, T_J=25°C	-	5	100	
		V_{IN} = VIN MAX, V_{OUT} = 0 V, V_{EN} = 0 V, V_{FCB} = 0 V, T_J=125°C	-	95	900	
I_{VDD}	Supply current into V_{DD}	V_{DD} > 3 V, I_{OUT} = 0 A, V_{EN} = 2 V, V_{FCB} = 2 V	-	125	350	uA
I_{VDDFL}	Supply current into V_{DD} when enabled at full load (ARPS1050A5)	V_{DD} > 3 V, I_{OUT} = I_{MAX}, V_{EN} = 2 V, V_{FCB} = 2 V, T_J=25°C	-	165	TBD	uA
		V_{DD} > 3 V, I_{OUT} = I_{MAX}, V_{EN} = 2 V, V_{FCB} = 2 V, T_J=125°C	-	270	TBD	
	Supply current into V_{DD} when enabled at full load (ARPS1020A5)	V_{DD} > 3 V, I_{OUT} = I_{MAX}, V_{EN} = 2 V, V_{FCB} = 2 V, T_J=25°C	-	180	TBD	
		V_{DD} > 3 V, I_{OUT} = I_{MAX}, V_{EN} = 2 V, V_{FCB} = 2 V, T_J=125°C	-	365	TBD	
I_{VIN_VDDO}	Supply current into V_{IN} when V_{DD} < 2 V, includes VIN to VOUT FET leakage	0 V ≤ V_{DD} ≤ 2 V, V_{EN} = 0 V, V_{FCB} = 0 V (ARPS1050A5)	-	155	700	uA
		0 V ≤ V_{DD} ≤ 2 V, V_{EN} = 0 V, V_{FCB} = 0 V (ARPS1020A5)	-	115	1100	
$TEMP_{SHUT}$	Over-temperature shutdown		130[(1)]	155	-	°C

(1) Guaranteed by design.

4.4 RADIATION RESILIENCE

For detailed radiation testing reports, please contact Apogee Semiconductor at support@apogeesemi.com.

Table 6: Radiation Resilience Characteristics

PARAMETER	CONDITIONS	VALUE	UNITS
Total Ionizing Dose (TID)	TID Radiation report to be published.	100	krad (Si)
SEB/SEGR Immune	ARPS1020A5, VIN = 20 V	72.8	MeV-cm^2/mg
	ARPS1050A5, VIN = 36 V		

5 TYPICAL CHARACTERISTICS

Figure 4 shows the series resistance R_{ON} of the ARPS1020A5 20 V device in mohms (mΩ).The data were collected at 25 °C with a 200 mA load current. Data from a single fabrication lot is shown.

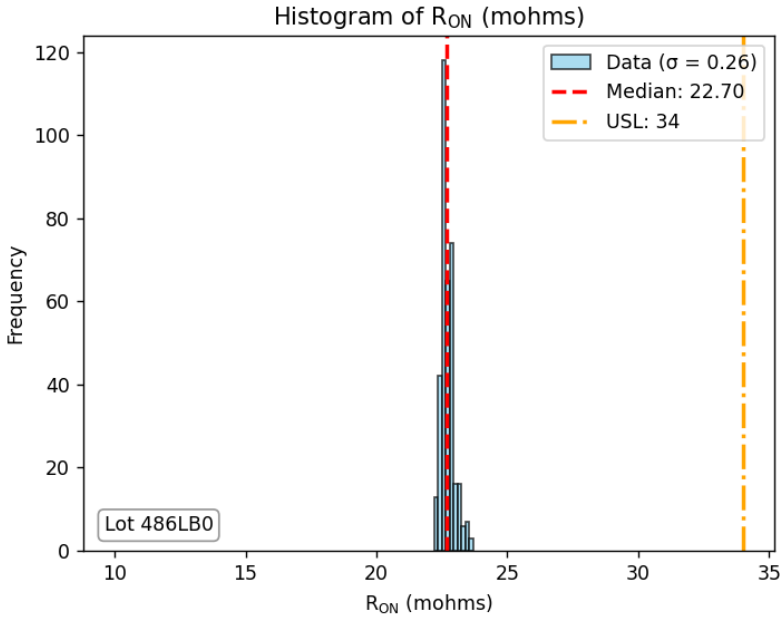

Figure 4: R_{ON} characterization of ARPS1020A5 20 V device in mohms (mΩ)

Figure 5 shows the series resistance R_{ON} of the ARPS1050A5 50 V device in mohms (mΩ). The data were collected at 25 °C with a 200 mA load current. Data from a single fabrication lot is shown.

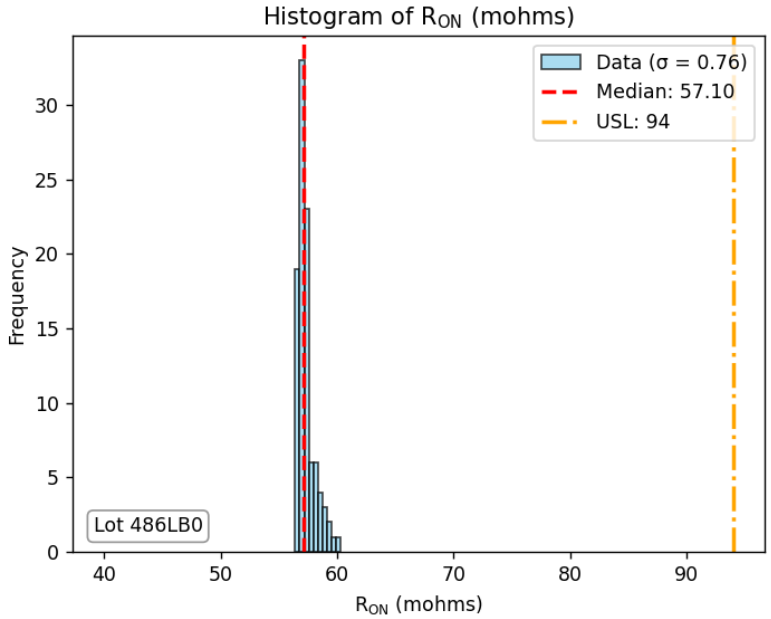

Figure 5: R_{ON} characterization of ARPS1050A5 50 V device in mohms (mΩ)

6 DETAILED DESCRIPTION

The ARPS1020A5 / ARPS1050A5 is a family of power switches. Each device is a single channel load switch with integrated power FET. Each device has an over-temperature trip and two current limit protection mechanisms.

- ARPS1020A5 contains a 20 V, 8 A, 23 mΩ RDSon, radiation-hardened power FET
- ARPS1050A5 contains a 50 V, 4 A, 57 mΩ RDSon, radiation-hardened power FET

6.1 FUNCTIONAL BLOCK DIAGRAM

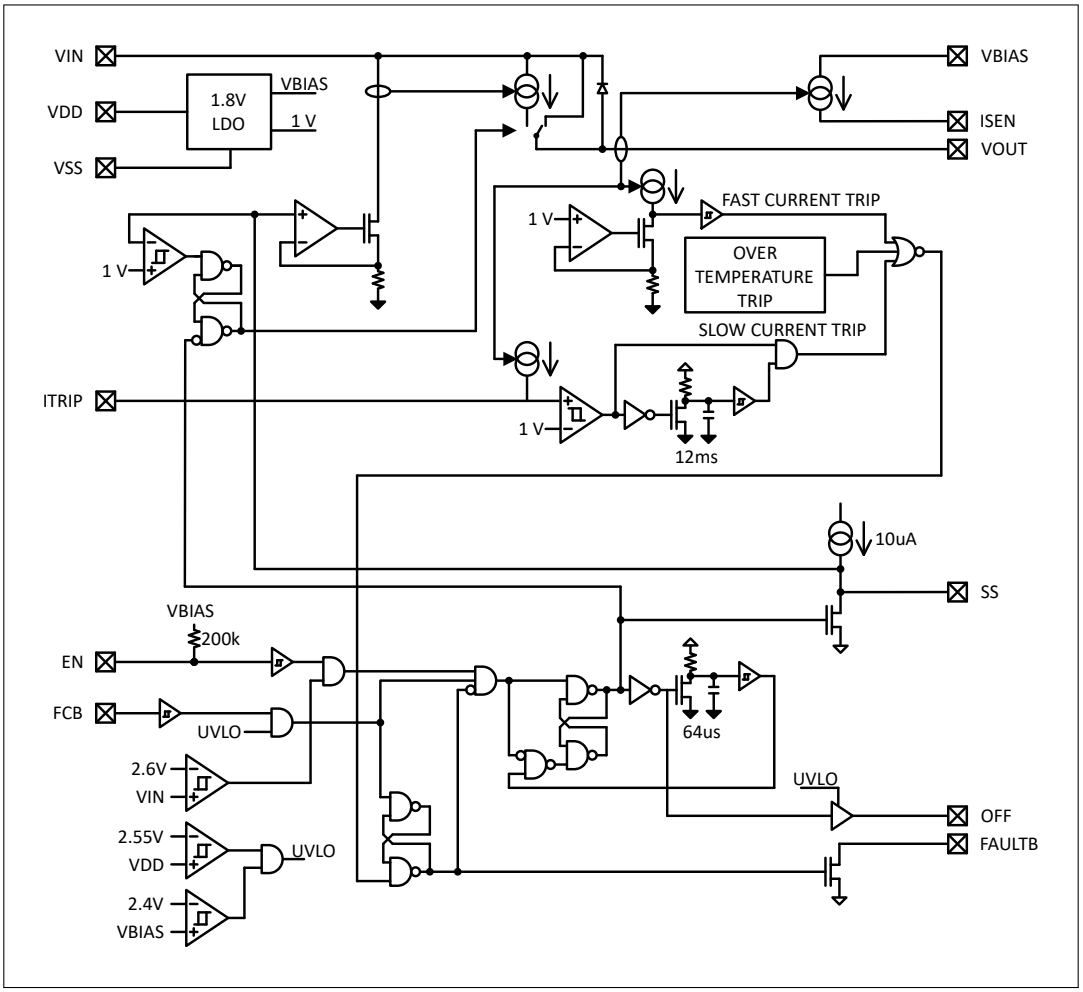

Figure 6: ARPS1020A5 / ARPS1050A5 Functional Block Diagram

6.2 VDD

The VDD pin provides input power to an internal low dropout regulator (LDO), which regulates the voltage on the VBIAS pin to a nominal 1.8 V. The VBIAS pin powers the majority of circuits within the IC and is also the voltage reference used internally. There should be nothing connected to the VBIAS pin other than a low ESR 220 nF capacitor. For stability, ensure that the capacitance is between 100 nF and 1 uF over tolerance, voltage, and temperature. It is possible to connect VDD directly to VIN to avoid needing a separate power supply for the device. It is also possible to power the VDD pin off any supply between 3.0 V and the maximum voltage allowed on VIN.

6.3 VIN

The VIN pin is the power supply which is switched to the VOUT pin.

6.4 POWER-ON RESET (POR)

There are PORs on the VDD, VBIAS and VIN. The device is powered through the VDD pin which must reach a voltage above $\mathbf{V_{DD\_START}}$. In addition, the VBIAS POR has to detect high enough VBIAS voltage in order for the internal circuits to operate and VIN must rise above $\mathbf{V_{IN\_START}}$ for the switch to be capable of being enabled.

If VIN drops below $\mathbf{V_{IN\_STOP}}$, the switch will be disabled and the capacitor on the SS pin will be discharged. The same behavior occurs when the EN pin had been lowered. In either case, the fault latch is not cleared.

If VDD drops below $\mathbf{V_{DD\_STOP}}$, the switch will be disabled AND the fault latch will be cleared (see Section 6.5 below) AND the capacitor on the SS pin will be discharge. This behavior is identical to that resulting from FCB being pulled low.

6.5 EN, FCB, AND OFF PINS

There are two input pins which must both be high to enable the output transistor: EN and FCB. These inputs are 5 V capable Schmitt trigger inputs which are powered off the VBIAS supply. The input levels are skewed to ensure that Vih and Vil levels are compatible with CMOS logic powered from a 1.5 V rail. Hence, they can be driven off any CMOS logic gate which is powered by a nominal 1.5 V to 5 V supply or from some resistor divider monitoring some other supply.

There is an internal latch which is set whenever a fault arises. This can be caused by a fast current trip, slow current trip, or an over-temperature condition. If the condition which caused the fault latch to be set is no longer present AND the FCB pin is pulled low, the fault latch is reset. The fault latch is also reset by the POR system (refer to Section 6.4 above).

The output switch will only turn on if FCB and EN are high, the fault latch has been reset, and the POR system detects high enough supply voltages to operate.

The OFF pin is a CMOS output which is driven high when the IC is powered up and the switching FET is in an off state. If the FET is currently in an on state or is transitioning to or from an on state, this pin is driven low. This can be used in conjunction with the EN and FCB pins to create a power switching circuit which can switch either of two supplies to a load, while ensuring break-before-make operation (see Section 7.1.3).

If any of the internal PORs is active, the OFF pin becomes high impedance. The EN pin has a nominal 200 kohms resistance pullup to VBIAS.

6.6 SOFT-START

The output voltage softstart is controlled by a capacitor between the SS pin and the VSS pin. When the switch is disabled, the SS pin is discharged to VSS. When the switch is enabled, a current of 10 uA charges the SS pin. Initially, the device outputs a maximum current proportional to the voltage on the SS pin $\mathrm{V_{SOFT\text{-}START}}$ per equation:

$$\mathrm{I_{SS\_OUT}} = \mathrm{K_{SS}} \times \mathrm{V_{SOFT\text{-}START}} \tag{1}$$

When the voltage on the SS pin exceeds 1 V, the power switch is quickly turned fully on.

The over-current protection circuits operate as normal both during soft-start and after the SS pin is fully charged.

By adjusting the capacitor on the SS pin, it is possible to limit the surge current that results from charging the capacitance on the VOUT pin. Larger capacitor on the SS pin reduces the surge current, but it will increase the time that soft-start takes and will increase the die temperature rise in the ARPS10x0x5 device. It is important

that the VOUT must be near fully charged by the time that the SS pin reaches 1 V, as the FET will rapidly be turned fully on at that time, which could result in a large surge current.

When the switch is disabled, the SS pin is discharged to VSS by an internal 50 ohm switch. To ensure adequate discharge of the SS pin before the power switch can be re-enabled, there is a timeout of between 32 us to 64 us implemented in the IC which prevents re-enabling of the switch until the SS capacitor is fully discharged.

In order to ensure full discharge of the capacitor on the SS pin, it is recommended that the maximum capacitance on the SS pin is no larger than 220 nF. If multiple devices are connected in parallel to the same capacitor on the SS pin, the max size of capacitance is 220 nF multiplied by the number of parallel devices.

To allow the designer to model the softstart operation, current draw and temperature rise in the device, a QSPICE model is available which fully models all of these behaviors.

When there is a fault condition or if the device is turned off via one or both of the EN and FCB pins being set low, there is no slew rate limiting when turning the power switch off.

6.7 I-SENSE

The IC measures the current flowing from Vin to Vout and outputs a scaled down replica of that current from the ISEN pin. This allows an external system to monitor the current flowing through the switch.

The ISEN pin current is calculated according to the following equation:

$$I_{ISENSE} = \frac{I_{VOUT}}{K_{ISENSE}} \tag{2}$$

6.8 FAULT PROTECTION

There are two over-current protection systems in the IC, a fast trip over-current and a slow trip over-current protection. There is also an over-temperature protection system.

The fast trip over-current protection is intended to protect the IC against damage when it attempts to power on the switch into a short on the VOUT pin. This protection is not customer programmable and is set at a high current threshold level, $\mathbf{I_{FAST}}$, so as to not trip during normal operation. The IC's fast current trip circuit is guaranteed to not trip for overcurrent events below 125% of $\mathbf{I_{MAX}}$. If the IC detects a current of greater than $\mathbf{I_{FAST}}$, it will turn off the switch in time $\mathbf{t_{IFAST}}$.

The slow trip over-current protection is intended to protect the external system from excessive currents on the load and is customer programmable. A current proportional to the current in the switch is output from the ITRIP pin. A customer selectable resistor, R_{ITRIP}, connected between the ITRIP pin and ground, converts the current to a voltage. When the voltage exceeds 1 V, the slow current trip is initiated.

The load current which will initiate trip. $\mathbf{I_{SLOW}}$ can be calculated according to the equation below:

$$I_{SLOW} = \frac{K_{ISLOW} \times 1\ V}{R_{ITRIP}} \tag{3}$$

This slow current trip is accurate over a range of values for R_{ITRIP} from 10 kohms to 100 kohms.

If an overcurrent beyond $\mathbf{I_{SLOW}}$ exists, an internal timer is started. If the overcurrent is present continuously for longer than time $\mathbf{t_{ISLOW}}$, the switch is turned off.

There is a thermal shutdown which measures the temperature of the silicon die. If the temperature rises above $\mathbf{TEMP_{SHUT}}$, again, the switch is turned off.

If the switch is turned off by any of the fault conditions, the FAULTB pin is pulled low to signal the fault to the external system. The latched FAULTB output can only be reset (cleared) by bringing the FCB pin low. In the case of a fault caused by an over-temperature trip, it is also necessary for the temperature to have fall below $\mathbf{TEMP_{SHUT}}$ before pulling FCB low to reset the fault latch.

7 APPLICATIONS

This section focuses on possible configurations using the ARPS10x0A5 family. In addition to these shown, an application note illustrates several use cases for the device in space power distribution and control systems (see ARPS1020A5/ARPS1050A5: Space Power Protection and Control Using Radiation-Hardened eFuses)

7.1 SAMPLE APPLICATION CONFIGURATIONS

Following are examples of configurations that are possible with the ARPS10x0A5 family of devices. Some of these configurations, including the single supply, dual supply, and parallel configurations, can be implemented and evaluated using the available Evaluation Board (EVB). For more information about the EVB or ordering one please refer to the Ordering Information Table or the ARPS10x0A5 Product Page.

7.1.1 Single Supply Configuration

Figure 7 shows the simplified schematic for a single supply configuration.

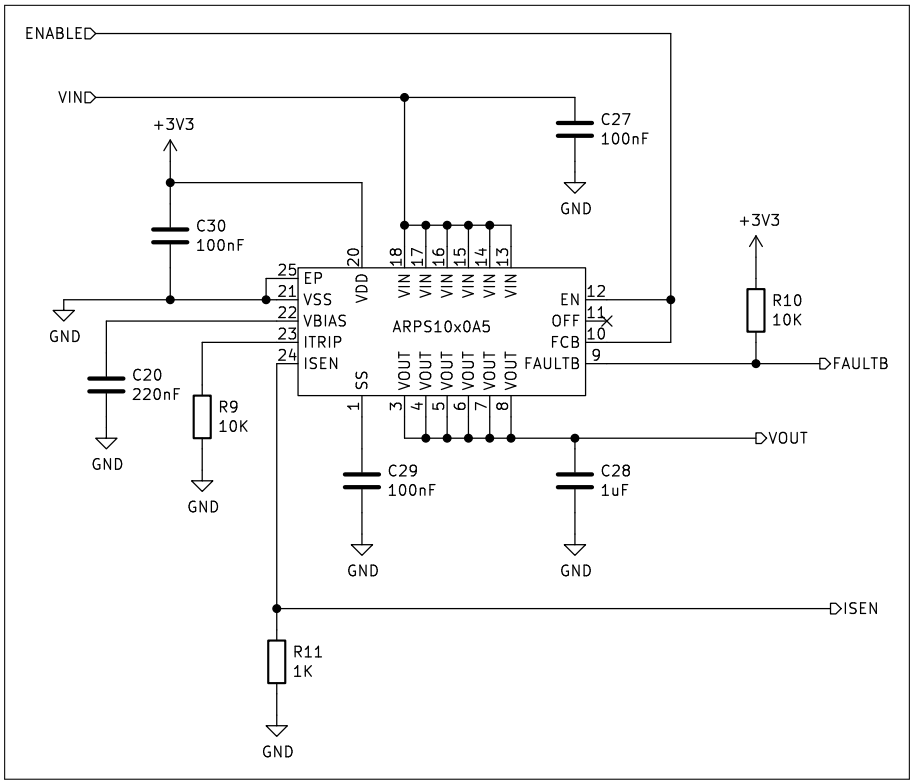

Figure 7: Single Supply Configuration

7.1.2 Transient Protection

In the case of a short-circuit, an overload current limit, or an over-temperature trip, the device interrupts current flow. The input inductance generates a positive voltage spike on the input, and the output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on the value of inductance in series with the input or output of the device as well as the proximity and size of capacitances on the VIN and VOUT pins. If such transients can exceed the absolute maximum ratings of the device, steps must be taken to address the issue. Figure 8 illustrates a transient protection circuit. Here, D3 is a transient voltage suppressor (TVS) and D4 is a Schottky diode.

If a TVS is needed on the input, it should be placed as close as possible to the VIN and GND pins to minimize inductance.

If a Schottky diode is needed on the output, it should be placed as close as possible to the VOUT and GND pins to minimize inductance.

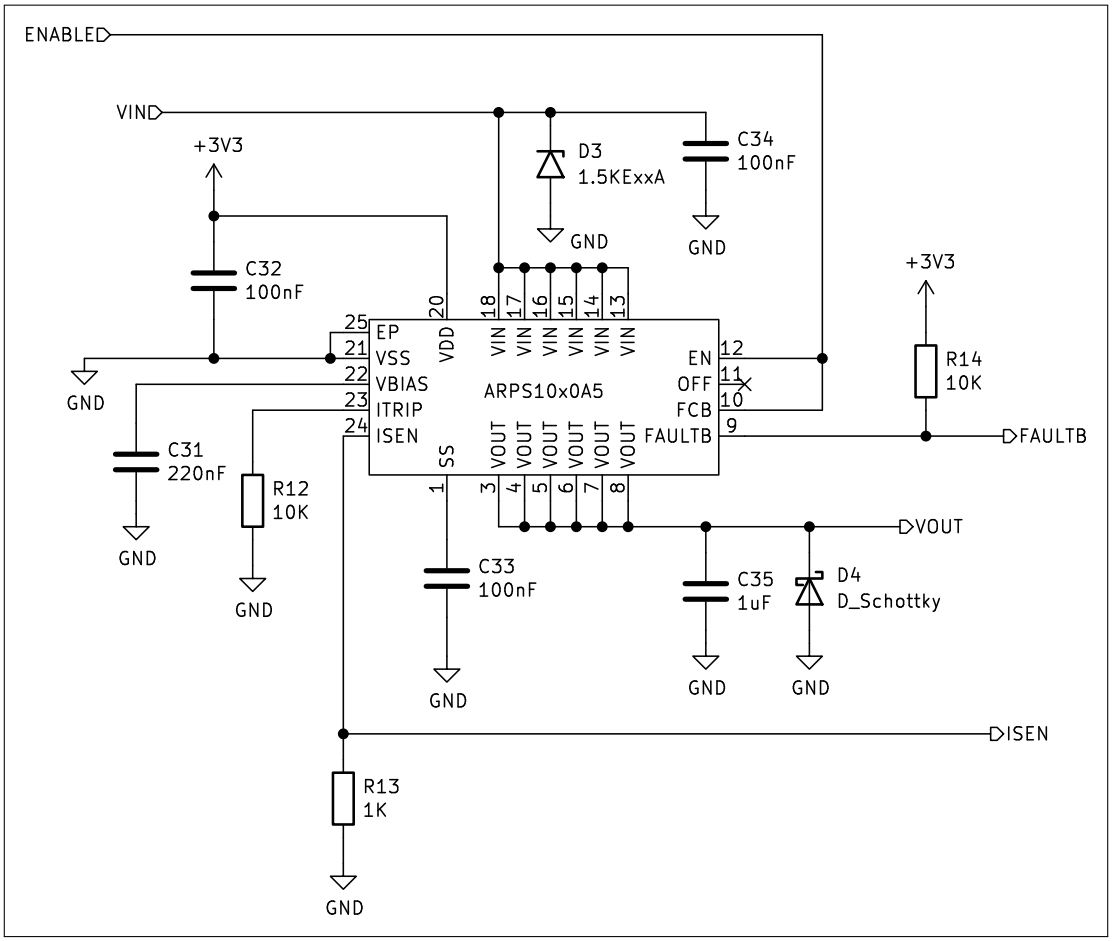

Figure 8: Single Supply Configuration with Transient Protection

7.1.3 Dual Supply Configuration

It is possible to connect two ARPS1020A5 or two ARPS1050A5 devices together with the addition of external reverse blocking diodes, to allow switching a load between two external power supplies (see Figure 9).

By use of the EN, FCB, and OFF pins, as shown in the example schematic, the circuit ensures that only one of the two ARPS10x0A5 devices is turned on at any given time. This ensures "break-before-make" operation.

To ensure proper break-before-make operation, the user should not assert both EN_VIN1 and EN_VIN2 simultaneously. If both switches are off and EN_VIN1 and EN_VIN2 are asserted nearly simultaneously, it is possible that the OFF signal on one or both of the devices will oscillate, and, further, neither switch will turn on. This state of oscillation will continue until one of the EN_VIN1 or EN_VIN2 signals is de-asserted, allowing the devices to determine which device the user wishes to turn on.

To eliminate the possibility of EN_VIN1 and EN_VIN2 being asserted simultaneously, the user should consider placing an Apogee Semiconductor arbiter fault containment part, the AP54RHC288, between the control system and the EN_VIN1 and EN_VIN2 signals in the application. This device will never pass two high signals received on the input to its output.

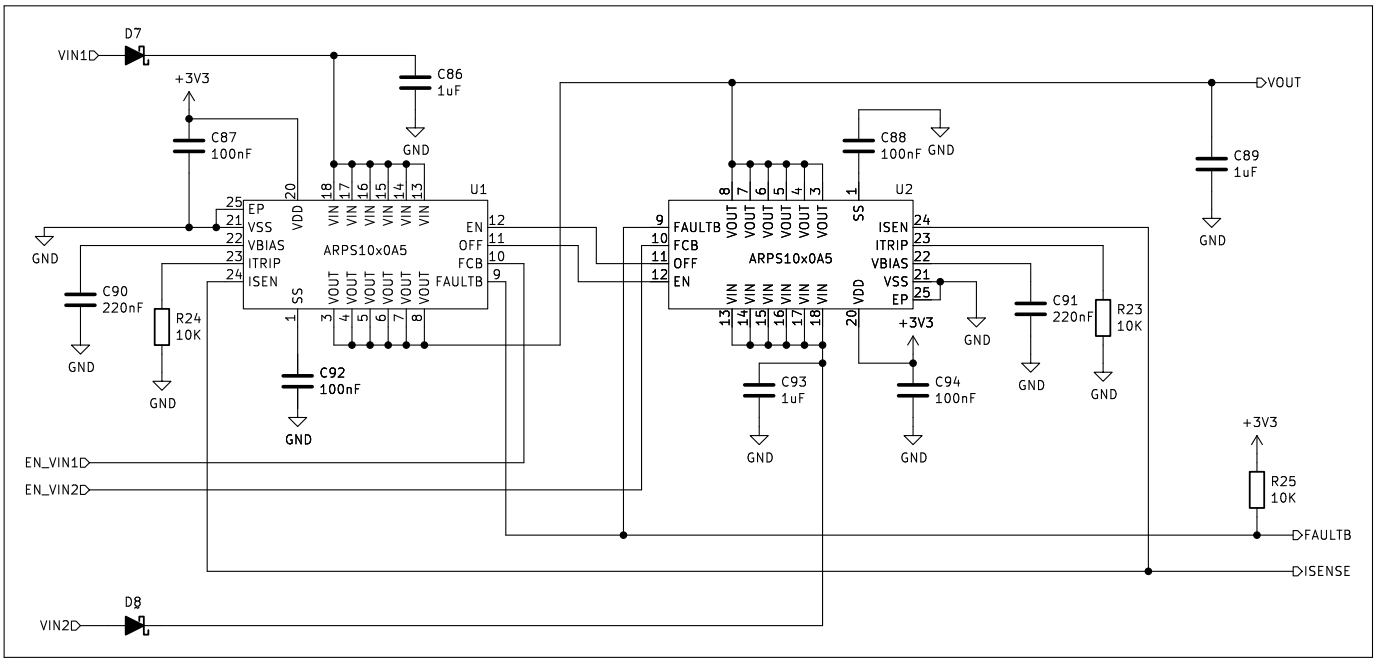

Figure 9: Dual Supply Configuration

7.1.4 Parallel Configuration

It is possible to connect multiple **ARPS1020A5 / ARPS1050A5** devices in parallel to reduce power dissipation and increase total current capacity when the devices are enabled (see Figure 10).

Current sharing of parallel devices depends on the matching of the ON resistance among devices and any variation in the voltage across the devices. It is important to ensure that the devices have similar ON resistance. This can be achieved by ensuring all devices connected in parallel are from the same silicon wafer lot (flight grade parts from the same reel). In addition, careful PCB and thermal layout is required, to ensure all devices see similar parasitic resistance in series with their VIN and VOUT paths from power supply and to load. The user must also ensure that the devices operate at a similar temperature, by mounting the devices in close proximity to each other and ensuring they are connected to the same heatsink, if one is used. The goal should be to operate the devices at no more than 10 °C temperature difference among devices operating with the same load.

The ON resistance matching achievable by adhering to these requirements is typically 1-3%. An example is shown in the following paragraphs.

As shown in the example application, all three devices connected in parallel have FAULTB pins connected together and connected to the EN pins, which is pulled up by the external control circuit. If ANY of the three ICs shuts down because of an over-temperature event or because of an overcurrent event, all three ICs will be disabled simultaneously via the FAULTB connection to the EN pins of all three ICs.

To clear the fault, the FCB pin must be pulled low. Once the fault has cleared, raising the FCB pins will re-enable all three ICs.

In addition, the SS pins of all the ICs are tied together to the same capacitor. This ensures that all the devices share power dissipation equally during soft-start, keeping the transient temperature rise in all devices similar to each other.

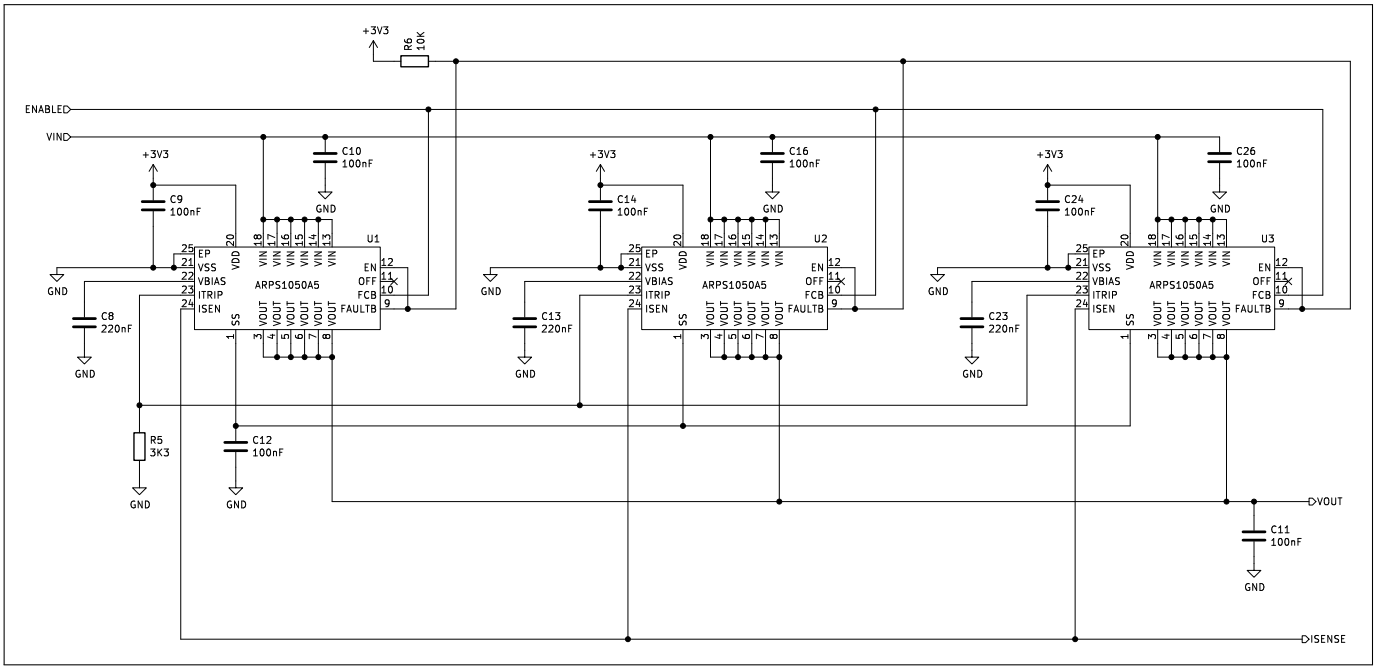

Figure 10: Parallel Configuration

The operation of two ARPS1050A5 devices in a parallel configuration is illustrated in Figure 11. Measurements were taken on an Apogee ARPS1050-S-EVB with two devices in parallel driving a 4.11 ohm load from 28 V. In the figure, the yellow and green traces show the current through each ARPS1050A5 into the load; the blue trace is the current difference between the two devices; and the orange trace is the shared SS pin voltage $V_{SOFT\text{-}START}$ (identical for

both devices). After the part is enabled, load current ramps in a controlled manner. The ratio of SS pin voltage $V_{SOFT\text{-}START}$ to load current follows K_{ISENSE} as specified in Table 5. For example, at $V_{SOFT\text{-}START} = 200\ mV$, the current per switch is approximately 1 A. Current rises smoothly to the steady-state value set by the condition $V_{OUT} \approx V_{IN}$ (at approximately 3.4 A per device in this case). In the example, when $V_{SOFT\text{-}START}$ reaches 0.8 V, the output capacitor is fully charged and V_{OUT} has reached steady state; this transition appears in the figure as a knee at approximately 5 ms. The small transient observed at 10 ms corresponds to the soft-start control loop being released which happens when $V_{SOFT\text{-}START}$ reaches 1 V. The IC design has margin for safe operation: if the load resistance decreases and demands more current, the soft-start knee shifts to the right (to higher current), up to a maximum current of 1.25× the maximum rated output current of the device before the soft-start control loop is disabled. Designers need to ensure that the soft-start capacitance chosen for an application allows the knee to occur before $V_{SOFT\text{-}START}$ reaches 1 V. If not, when $V_{SOFT\text{-}START}$ reaches 1 V the FETs will be rapidly enabled and V_{OUT} will be rapidly charged in an uncontrolled way, resulting in a large in-rush current. In steady-state, the current imbalance between the two devices approaches 43 mA against a total load current of 6.8 A, corresponding to matching within ±1% (43 mA/6.8 A < 1%). The devices used on the board were randomly taken from a distribution of devices similar to the histogram data in Section 5. This level of matching is within the expected level for any two devices from the same wafer lot (which is guaranteed for flight grade parts within a reel).

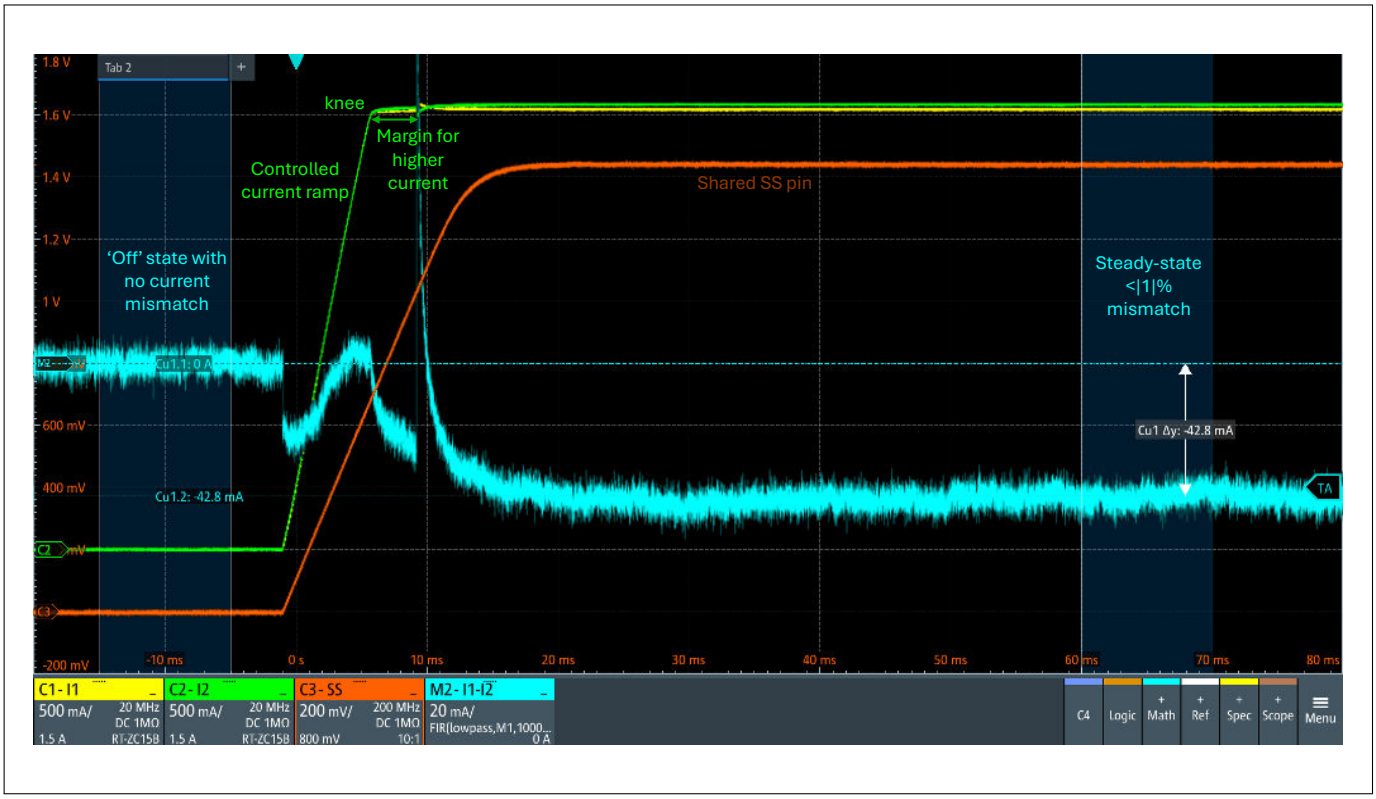

Figure 11: Soft-Start Waveform

7.1.5 Parallel Dual Supply Configuration

It is possible to connect multiple **ARPS1020A5 / ARPS1050A5** devices in parallel to reduce power dissipation and increase total current capacity and then connect the paralleled devices to switch between two power supplies (see Figure 12).

In the example shown, three devices are connected in parallel per power supply.

Because parallel devices should be from the same wafer lot, they will match each other very closely. It is sufficient to use the "OFF" output from one of the parallel devices in a bank to signal to the other bank of parallell devices that the whole bank is "OFF".

Note that the "OFF" signal from one bank passes through a resistor and the FAULTB and EN signals from all the devices in the other bank are shorted to the other end of the resistor. This means that the other bank of devices will all turn off if any of them have a fault. Also, all devices in a bank will turn on or turn off at the same time.

In addition, the SS pins of all the ICs in each bank are tied together to the same capacitor. This ensures that all the devices share power dissipation equally during soft-start, keeping the transient temperature rise in all devices similar to each other.

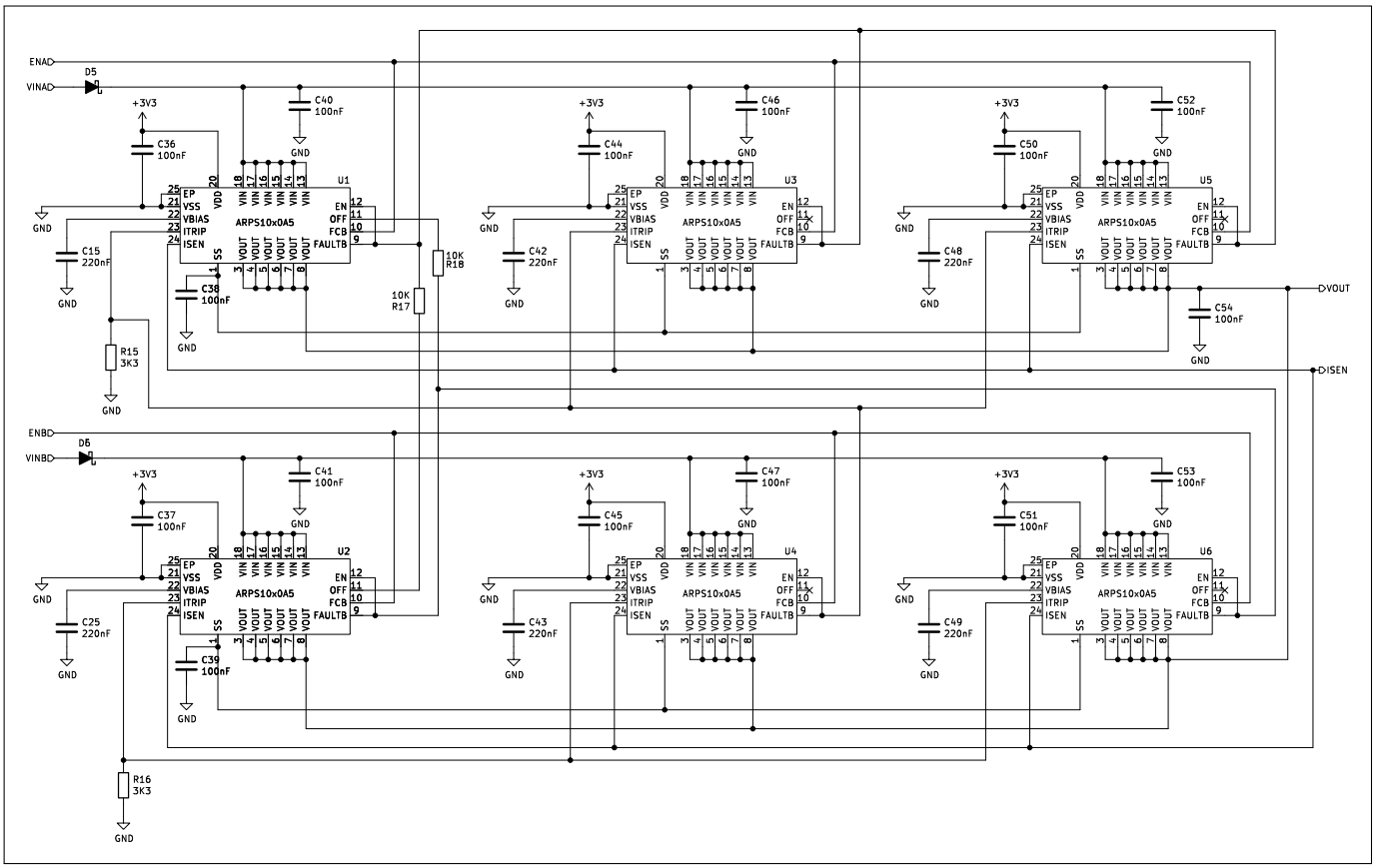

Figure 12: Parallel Dual Supply Configuration

7.2 APPLICATION GUIDELINES

The EN, FCB, and FAULTB pins of the IC are very robust to single event effects (SEE), however, it may be desirable to "majority vote" the control signals EN and/or FCB in order to mask erroneous instructions from the external system. This can be achieved by using the Apogee part number AP54RHC301, a dual 3-input majority voter.

If it is desired to control multiple ICs, users might consider controlling the ICs using Apogee's radiation-hardened GPIO expander, the APIO16 or AFIO16.

7.3 LAYOUT GUIDELINES

Optimal placement of input decoupling capacitor on VIN is closest to the VIN and VSS pins of the device. Optimal placement of output decoupling capacitor on VOUT is closest to the VOUT and VSS pins of the device. A 220 nF decoupling capacitor should be placed as close as possible between the VBIAS pin and VSS.

If multiple devices are to be connected in parallel the following conditions should be observed to ensure close matching of current among devices:

- All parallel devices should be from the same wafer lot.
- All parallel devices should be wired up such that they all see similar resistance in the VIN and VOUT paths.
- All parallel devices should see similar voltage on their VSS pins, to ensure close tracking of soft-start operation.
- All parallel devices should operate in a similar temperature environment, to ensure close matching of temperature (within 10 °C).
- All parallel devices should have their EN and FAULTB pins connected together to the same single node, with a pullup resistor. This ensures that if one device shuts down through a fault, they all shut down. All devices should have their SS pins shorted together to ensure tracking during soft-start.

8 PACKAGING INFORMATION

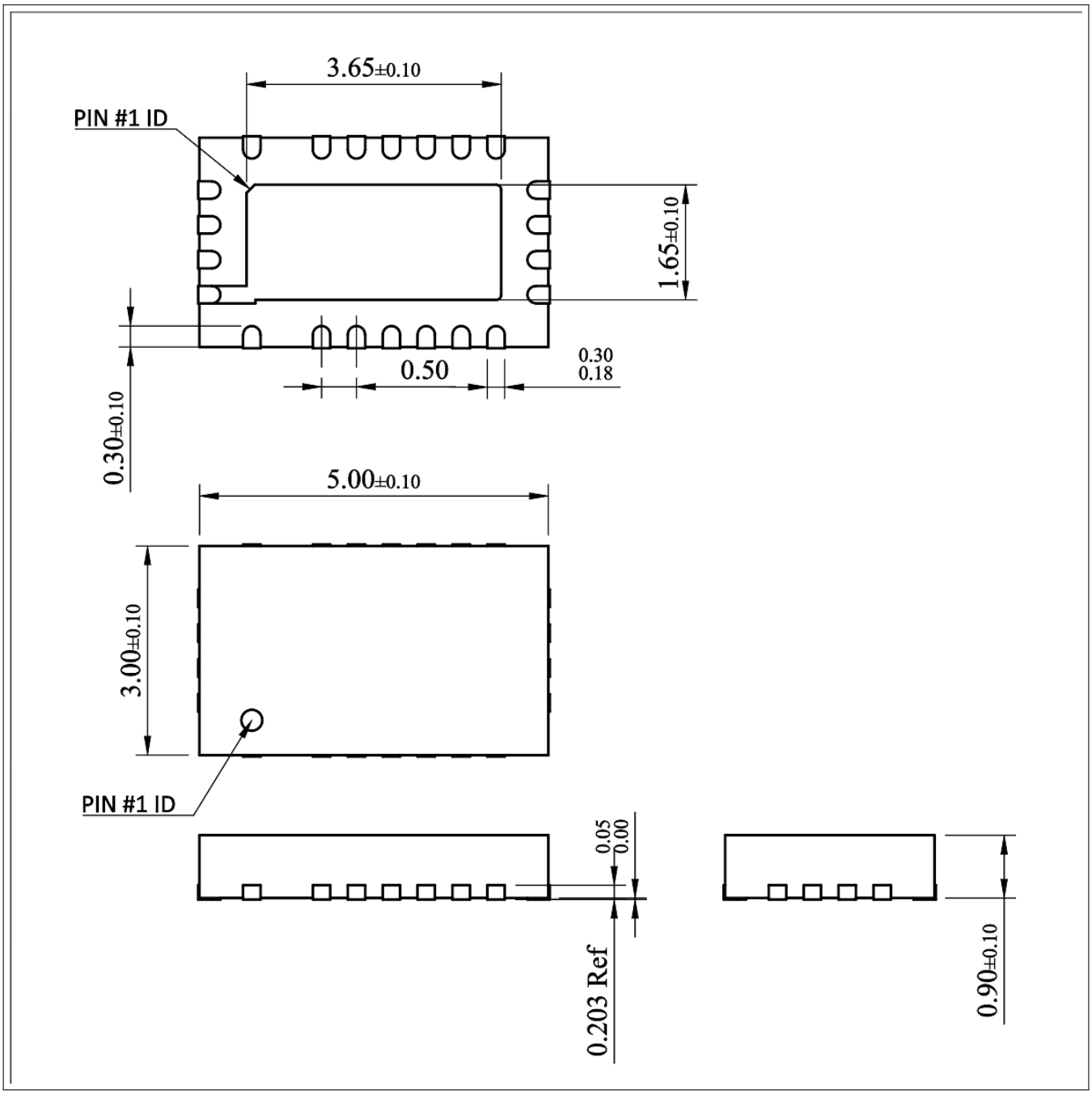

Figure 13: Mechanical Detail of 24-Pin QFN Package

Notes:

(1) All linear dimensions are in millimeters.

9 ORDERING INFORMATION

Orderable part numbers (OPNs) for the ARPS1020A5 / ARPS1050A5 are listed in Table 7. The part number decoder detailing the options for this part can be found in Figure 14. Please contact Apogee Semiconductor sales at sales@apogeesemi.com for further information on sampling, lead times, and purchasing specific part numbers including the ARPS10x0-x-EVB.

Table 7: ARPS1020A5 / ARPS1050A5 Ordering Information Table

DEVICE	DESCRIPTION	PACKAGING	PACKAGE	LEAD FINISH	STATUS
ARPS1020A5ANQ-R	Radiation Hardened eFuse 20 V / 8 A, A-Grade Flight (LEO/GEO)	Reel	QFN	NiPdAu	Plan Rls JUN-2026
ARPS1020A5ANQ-J (1)		Tray			
ARPS1020A5BNQ-R	Radiation Hardened eFuse 20 V / 8 A, B-Grade Flight (LEO/GEO)	Reel	QFN	NiPdAu	Plan Rls JUN-2026
ARPS1020A5BNQ-J (1)		Tray			
ARPS1020A5CNQ-R	Radiation Hardened eFuse 20 V / 8 A, C-Grade Flight (LEO/GEO)	Reel	QFN	NiPdAu	Plan Rls JUN-2026
ARPS1020A5CNQ-J (1)		Tray			
ARPS1020A5ENQ-R (2)	Radiation Hardened eFuse 20 V / 8 A, E-Grade (Evaluation Only)	Reel	QFN	NiPdAu	Available
ARPS1020A5ENQ-J (1)		Tray			
ARPS1050A5ANQ-R	Radiation Hardened eFuse 50 V / 4 A, A-Grade Flight (LEO/GEO)	Reel	QFN	NiPdAu	Plan Rls JUN-2026
ARPS1050A5ANQ-J (1)		Tray			
ARPS1050A5BNQ-R	Radiation Hardened eFuse 50 V / 4 A, B-Grade Flight (LEO/GEO)	Reel	QFN	NiPdAu	Plan Rls JUN-2026
ARPS1050A5BNQ-J (1)		Tray			
ARPS1050A5CNQ-R	Radiation Hardened eFuse 50 V / 4 A, C-Grade Flight (LEO/GEO)	Reel	QFN	NiPdAu	Plan Rls JUN-2026
ARPS1050A5CNQ-J (1)		Tray			
ARPS1050A5ENQ-R (2)	Radiation Hardened eFuse 50 V / 4 A, E-Grade (Evaluation Only)	Reel	QFN	NiPdAu	Available
ARPS1050A5ENQ-J (1)		Tray			
ARPS1020-S-EVB (2)	EVB E-Grade High-Side Switch 20 V / 8 A Single (Evaluation Only)	-	EVB	-	Available
ARPS1020-D-EVB (2)	EVB E-Grade High-Side Switch 20 V / 8 A Dual (Evaluation Only)				
ARPS1050-S-EVB (2)	EVB E-Grade High-Side Switch 50 V / 4 A Single (Evaluation Only)				
ARPS1050-D-EVB (2)	EVB E-Grade High-Side Switch 50 V / 4 A Dual (Evaluation Only)				

(1) Available through distributors only.

(2) E-grade devices available now are X marked. E-Grade devices with an X preceding the date code (YYWW) are not the production version of the product. X marked products will be sold only when a device is in pre-production status (see Product Grades and Quality Flows).

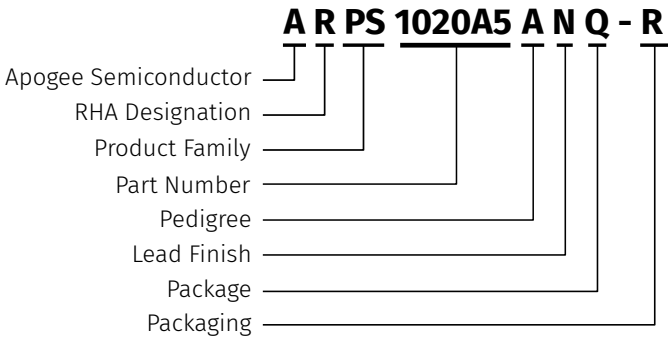

Figure 14: Part Number Decoder

1. RHA Designation
   - **R** 100 krad (Si)
2. Product Family
   - **PS** Power Switch
3. Part Number
   - **1020A5** 20 V / 8 A
   - **1050A5** 50 V / 4 A
4. Pedigree
   - **A** -55 to +125 °C (Burn-in)
   - **B** -55 to +125 °C (No burn-in)
   - **C** 25 °C (No burn-in)
   - **E** 25 °C Functional Test Only (Evaluation)
5. Lead Finish
   - **N** Nickel Palladium Gold (NiPdAu)
6. Package
   - **Q** QFN Package
7. Packaging
   - **W** Waffle Pack or Pillow Stat Box
   - **R** Tape and Reel[(1)]
   - **J** JEDEC Tray

[(1)] Contact us for custom reel quantities. Orders less than full reel quantities may be shipped as cut tape.

10 REVISION HISTORY

REVISION	DESCRIPTION	DATE
B02	Fixed error in pin description for EN and FCB pins	April 1, 2026
B01	Added histograms of Ron for 20 V and 50 V parts. Updated EVB orderable part numbers. Updated SEB/SEGR LET value from 72 MeV-cm^2/mg to 73 MeV-cm^2/mg.	March 19, 2026
B00	Initial internal release.	February 16, 2026

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2. Pre-production — Status at the time of E grade release to market. Specifications are supported by simulation and initial device characterization, with few to no TBDs. Limits are not yet finalized and may change prior to Production release.

3. Production — Status at the time of flight grade release to market. This is a final, controlled datasheet with confirmed specifications, performance metrics, and compliance information verified through qualification and production test. Any future specification updates will follow the formal PCN (Product Change Notification) process.