Radiation-Hardened 5-Channel Level Translator

with **cold sparing** and **bus-keeper**

1 GENERAL DESCRIPTION

The **AP54RHC505** is a radiation-hardened by design **5-channel level translator with 3-state outputs and bus-keepers** that is ideally suited for commercial space and other applications demanding radiation tolerance and high reliability. It is fabricated in a 180 nm CMOS process utilizing proprietary radiation-hardening techniques, delivering high resiliency to single-event effects (SEE) and to a total ionizing dose (TID) up to **30 krad (Si) at 5 V** and **70 krad (Si) at 3.3 V**.

This device is a member of the Apogee Semiconductor AP54RHC logic family. All members of this family operate across a full **1.65 V to 5.5 V** range providing the system designer flexibility in logic-level interfaces. The AP54RHC505 can operate across this range on both of its supply voltage inputs, $V_{CC}A$ and $V_{CC}Y$.

An output enable control pin allows the outputs to be placed in a high impedance (high-Z) state, simplifying usage in applications with shared busses or mixed power domains. Additionally, the outputs are placed in high-Z when $V_{CC}A$ and $V_{CC}Y$ is not present, ensuring that no loading or leakage paths are experienced at the output nodes when the power rail are not powered.

Zero-power penalty™ cold sparing is supported, along with Class 2 ESD protection on all inputs and outputs. A proprietary output stage and robust power-on reset (POR) circuit allow the AP54RHC505 to be cold-spared in any redundant configuration with no static power loss on any pad of the device. The redundant output stage also features a high drive capability with low static power loss.

The AP54RHC505 also features a triple-redundant design throughout its entire circuitry, which allows it to be immune to single-event transients (SET) without requiring additional redundant devices.

Ordering information may be found in Table 10 on Page 15.

1.1 FEATURES

- **1.65 VDC to 5.5 VDC** operation
- Inputs tolerant up to 5.5 VDC at any $V_{CC}A$ or $V_{CC}Y$
- Bus-keep on inputs and outputs eliminates needs for pullup/down biasing
- All bus-keep circuitry is disabled during POR for cold sparing
- Extended operating temperature range (-55 °C to +125 °C)
- Proprietary **cold sparing capability** with **zero** static power penalty
- **Built-in triple redundancy** for enhanced reliability
- Class 2 ESD protection (4000 V HBM, 500 V CDM)
- TID resilience of **30 krad (Si)** assured at 5.5 V and characterized to **70 krad (Si)** at 3.3 V
- SEL immune to LET of **80 MeV-cm^2/mg**
- Meets NASA's ASTM E595 outgassing specification

1.2 LOGIC DIAGRAM

The AP54RHC505 logic function is shown below:

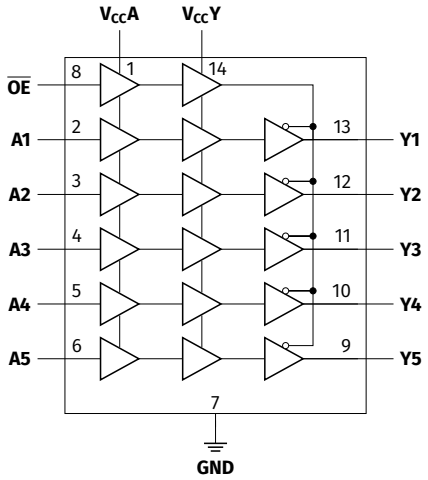


Figure 1: AP54RHC505 Logic Diagram

CONTENTS

LIST OF TABLES

LIST OF FIGURES

2 ACRONYMS AND ABBREVIATIONS

ESD	Electrostatic Discharge
POR	Power On Reset
RHA	Radiation Hardness Assurance
SEE	Single Event Effects
SEL	Single Event Latchup
SET	Single Event Transient
TID	Total Ionizing Dose
TMR	Triple Modular Redundancy
CDM	Charged-device Model
HBM	Human-body Model

3 LOGIC DATA

The AP54RHC505 truth table is found in Table 1. **H** indicates HIGH logic level, **L** indicates LOW logic level, **X** indicates DON'T CARE and **Z** indicates HIGH-Z (TRI-STATE). Subscript **n** reflects one of the five buffers in the device (1 to 5).

Table 1: AP54RHC505 Device Truth Table

Supplies	Inputs		Output
$V_{CC}A$ and $V_{CC}Y$	$\overline{OE}$	A_n	Y_n
Unpowered	X	X	Z
Powered	H	X	Z
Powered	L	L	L
Powered	L	H	H

4 PIN CONFIGURATION

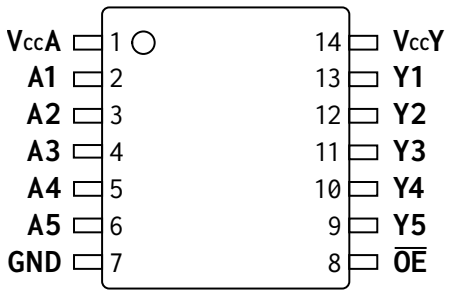


Figure 2: AP54RHC505 Device Pinout

Table 2: AP54RHC505 Device Pinout

PIN NAME(S)	PIN NUMBER(S)	DESCRIPTION
A1 A2 A3 A4 A5	2 3 4 5 6	Signal Inputs. Referenced to $V_{CC}A$.
Y1 Y2 Y3 Y4 Y5	13 12 11 10 9	Signal Outputs. Referenced to $V_{CC}Y$.
$\overline{OE}$	8	Output Enable (active-low). Referenced to $V_{CC}A$.
$V_{CC}A$	1	Positive Voltage Supply (A Side)
$V_{CC}Y$	14	Positive Voltage Supply (Y Side)
GND	7	Ground

5 ELECTRICAL CHARACTERISTICS

The sign convention for current follows JEDEC standards with negative values representing current sourced from the device and positive values representing current sunk into the device.

5.1 ABSOLUTE MAXIMUM RATINGS

Excursions beyond the values listed in Table 3 may cause permanent damage to the device. Proper function of the device cannot be guaranteed if these values are exceeded, and long-term device reliability may be affected. Functionality of the device at these values, or beyond those listed in Recommended Operating Conditions (Table 4) is not guaranteed.

All parameters are specified across the entire operating temperature range unless otherwise specified.

Table 3: Absolute Maximum Ratings

SYMBOL	PARAMETER		VALUE	UNITS
$V_{CC}A$, $V_{CC}Y$	Supply Voltage		-0.5 to +5.5	V
V_I	Input voltage range		-0.5 to +5.5	V
V_O	Output voltage range		-0.5 to $V_{CC}Y$ + 0.5[1]	V
I_{IK} (V_I < 0)	Input clamp current		100	mA
I_O	Continuous output current (per pin)		100	mA
I_{CC}	Maximum supply current		100	mA
V_{ESD}	ESD Voltage	HBM	4000	V
		CDM	500	V
T_J	Operating junction temperature range		-55 to +150	°C
T_{STG}	Storage temperature range		-65 to +150	°C

(1) V_O must remain below absolute maximum rating of $V_{CC}A$, $V_{CC}Y$

5.2 RECOMMENDED OPERATING CONDITIONS

All recommended parameters below are specified across the entire operating temperature range unless otherwise specified.

Table 4: Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	MAX	UNITS
$V_{CC}A$, $V_{CC}Y$	Supply voltage		1.65	5.5	V
V_I	Input voltage range		0	5.5	V
V_O	Output voltage range		0	$V_{CC}Y$	V
V_{IH}	HIGH-level input voltage	$V_{CC}A$ = 1.65 to 1.95 V	1.4	-	V
		$V_{CC}A$ = 2.3 to 2.7 V	1.9	-	
		$V_{CC}A$ = 3.0 to 3.6 V	2.5	-	
		$V_{CC}A$ = 4.5 to 5.5 V	3.8	-	
V_{IL}	LOW-level input voltage	$V_{CC}A$ = 1.65 to 1.95 V	-	0.4	V
		$V_{CC}A$ = 2.3 to 2.7 V	-	0.6	
		$V_{CC}A$ = 3.0 to 3.6 V	-	0.9	
		$V_{CC}A$ = 4.5 to 5.5 V	-	1.35	
I_{OH}	HIGH-level output current	$V_{CC}Y$ = 1.65 to 1.95 V	-	-4	mA
		$V_{CC}Y$ = 2.3 to 2.7 V	-	-8	
		$V_{CC}Y$ = 3.0 to 3.6 V	-	-16	
		$V_{CC}Y$ = 4.5 to 5.5 V	-	-24	
I_{OL}	LOW-level output current	$V_{CC}Y$ = 1.65 to 1.95 V	-	4	mA
		$V_{CC}Y$ = 2.3 to 2.7 V	-	8	
		$V_{CC}Y$ = 3.0 to 3.6 V	-	16	
		$V_{CC}Y$ = 4.5 to 5.5 V	-	24	
t_r, t_f	Input rise or fall time (10% - 90%)	$V_{CC}A$ = 1.65 to 1.95 V	-	1000	ns
		$V_{CC}A$ = 2.3 to 2.7 V	-	600	
		$V_{CC}A$ = 3.0 to 3.6 V	-	500	
		$V_{CC}A$ = 4.5 to 5.5 V	-	400	

Table 5: Thermal Information

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
T_J	Operating junction temperature	-55	-	+125	°C
$R_{\theta JA}$	Junction to ambient thermal resistance	-	100	-	°C/W

5.3 STATIC CHARACTERISTICS

All parameters are specified across the entire operating temperature range unless otherwise specified.

Table 6: DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	$V_{CC}Y$	MIN	TYP	MAX	UNITS
V_{OL}	LOW-Level Output Voltage[1]	I_O = 100 µA	1.65 to 5.5 V	-	0.02	0.05	V
		I_O = 1 mA	1.65 to 5.5 V	-	0.05	0.15	V
		I_O = 4 mA	1.65 V	-	0.27	0.8	V
			2.3 V	-	0.3	0.6	V
			3.0 V	-	0.2	0.4	V
			4.5 V	-	0.2	0.4	V
		I_O = 8 mA	2.3 V	-	0.6	1.0	V
			3.0 V	-	0.4	0.8	V
			4.5 V	-	0.3	0.6	V
		I_O = 16 mA	3.0 V	-	1.0	1.4	V
			4.5 V	-	1.1	1.2	V
		I_O = 24 mA	4.5 V	-	1.1	1.5	V
V_{OH}	HIGH-Level Output Voltage[1]	I_O = -100 µA	1.65 to 5.5 V	$V_{CC}Y$ - 0.1	$V_{CC}Y$ - 0.02	-	V
		I_O = -1 mA	1.65 to 5.5 V	$V_{CC}Y$ - 0.15	$V_{CC}Y$ - 0.08	-	V
		I_O = -4 mA	1.65 V	1	1.35	-	V
			2.3 V	1.8	2.0	-	V
			3.0 V	2.6	2.8	-	V
			4.5 V	4.2	4.4	-	V
		I_O = -8 mA	2.3 V	1.4	1.7	-	V
			3.0 V	2.2	2.5	-	V
			4.5 V	3.9	4.1	-	V
		I_O = -16 mA	3.0 V	1.5	2.0	-	V
			4.5 V	3.3	3.8	-	V
		I_O = -24 mA	4.5 V	3.0	3.5	-	V
$I_{CC}Y$	Quiescent supply current	V_I = $V_{CC}A$ or GND $\overline{OE}$ = GND I_O = 0 mA	5.5 V	-	100	150	µA

[1] $V_{CC}A$ = 1.65 to 5.5 V for these conditions

SYMBOL	PARAMETER	$V_{CC}A$	CONDITIONS	MIN	TYP	MAX	UNITS
I_I	Input current	1.65 to 5.5 V	V_I = 5.5 V or GND	-	-	±1	µA
I_{OZ}	Output leakage current(1)	1.65 to 5.5 V	V_I = 5.5V or GND $\overline{OE}$ = $V_{CC}A$	-	-	±2.5	µA
I_{OFF}	Powerdown leakage current(2)	OFF	V_I = GND to 5.5 V	-	-	5	µA
$I_{CC}A$	Quiescent supply current	5.5 V	V_I = $V_{CC}A$ or GND I_O = 0 mA	-	13	30	µA
I_{bh} (Hold)	Bus-keep Sustaining Current	1.8 ±0.15 V	V_I = 0.4 V	4.1	5.7	-	µA
			V_I = 1.4V	-	-5.7	-2.5	µA
		2.5 ±0.2 V	V_I = 0.6V	6.1	8.5	-	µA
			V_I = 1.9 V	-	-8.5	-4.1	µA
		3.3 ±0.3 V	V_I = 0.9 V	9.2	12.8	-	µA
			V_I = 2.5 V	-	-11.4	-5.1	µA
		5 ±0.5 V	V_I = 1.35 V	13.8	19.2	-	µA
			V_I = 4.4 V	-	-17	-7.1	µA
$\lvert I_{bo} \rvert$	Bus-keep Maximum Overdrive Current	1.8 ±0.15 V	V_I = 0 to 1.95 V	-	25.5	39.8	µA
		2.5 ±0.2 V	V_I = 0 to 2.7 V	-	35.5	55.1	µA
		3.3 ±0.3 V	V_I = 0 to 3.6 V	-	46.8	73.5	µA
		5 ±0.5 V	V_I = 0 to 5.5 V	-	71	112	µA

(1) $V_{CC}Y$ = GND to 5.5 V for these conditions.
(2) $V_{CC}A$ and $V_{CC}Y$ are at GND potential

5.4 DYNAMIC CHARACTERISTICS

All parameters are specified across the entire operating temperature range unless otherwise specified.

Table 7: AC Electrical Characteristics. C_L = 50 pF

Symbol	Parameter	$V_{CC}A$	$V_{CC}Y$ 1.8 ±0.15 V		$V_{CC}Y$ 2.5 ±0.2 V		$V_{CC}Y$ 3.3 ±0.3 V		$V_{CC}Y$ 5 ±0.5 V		Units
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
t_{pd}[1]	Propagation Delay (Input **A** to Output **Y**)	1.8 ±0.15 V	11.8	25	7.9	15	6.2	13	5.8	11	ns
		2.5 ±0.2 V	11.3	25	7.4	15	5.6	13	4.3	11	ns
		3.3 ±0.3 V	11.2	25	7.2	15	5.4	13	4	11	ns
		5 ±0.5 V	11.1	25	7.1	15	5.3	13	3.9	11	ns
t_{dis}[2]	Output Disable Time (Input $\overline{\textbf{OE}}$ to Output **Y**)	1.8 ±0.15 V	18.3	53	17.2	41	17.1	35	18.2	25	ns
		2.5 ±0.2 V	17.9	53	16.7	41	16.3	35	16.2	25	ns
		3.3 ±0.3 V	17.7	53	16.6	41	16.1	35	15.9	25	ns
		5 ±0.5 V	17.7	53	16.5	41	16.1	35	15.9	25	ns
t_{en}[3]	Output Enable Time (Input $\overline{\textbf{OE}}$ to Output **Y**)	1.8 ±0.15 V	21.7	53	17.3	41	15.5	35	15.1	25	ns
		2.5 ±0.2 V	21.4	53	16.9	41	15.0	35	13.7	25	ns
		3.3 ±0.3 V	21.3	53	16.8	41	14.9	35	13.5	25	ns
		5 ±0.5 V	21.4	53	17.0	41	15.0	35	13.6	25	ns

(1) equivalent to t_{PLH}, t_{PHL}
(2) equivalent to t_{PLZ}, t_{PHZ}
(3) equivalent to t_{PZL}, t_{PZH}

Table 8: AC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	$V_{CC}Y$	MIN	TYP	MAX	UNITS
t_{sk}	Channel-to-channel skew	C_L = 50 pF	1.65 to 5.5 V	-	-	1	ns
C_{in}	Input Capacitance[1]	V_I = V_{CC} or GND	1.65 to 5.5 V	-	2	4	pF
C_{pd}	Power Dissipation Capacitance[1]	I_O = 0 mA, f = 1 MHz	5.5 V	-	40	-	pF

(1) guaranteed by design

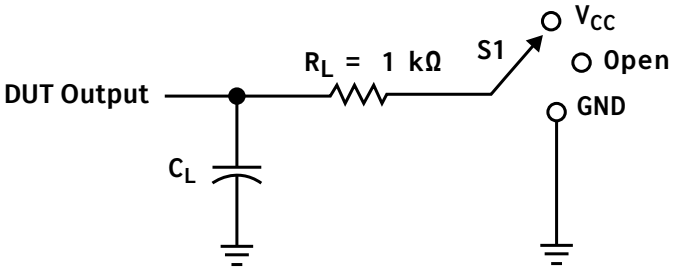
5.5 RADIATION RESILIENCE

For detailed radiation testing reports, please contact Apogee Semiconductor at sales@apogeesemi.com.

Table 9: Radiation Resilience Characteristics

PARAMETER	CONDITIONS	VALUE	UNITS
Total Ionizing Dose (TID)	Please contact Apogee Semiconductor for test report.	30	krad (Si)
SEL Onset LET Threshold	Please contact Apogee Semiconductor for test report.	≥80	MeV-cm^2/mg

5.6 CHARACTERISTICS MEASUREMENT INFORMATION



TEST	S1
t_{pd}	GND
t_{PLZ}, t_{PZL}	V_{CC}
t_{PHZ}, t_{PZH}	GND

Figure 3: Load Circuit for 3-State Outputs

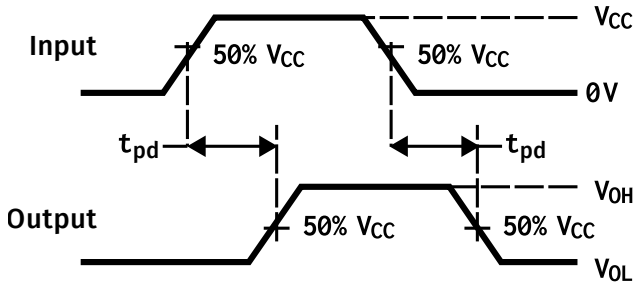


Figure 4: Propagation Delay Measurement

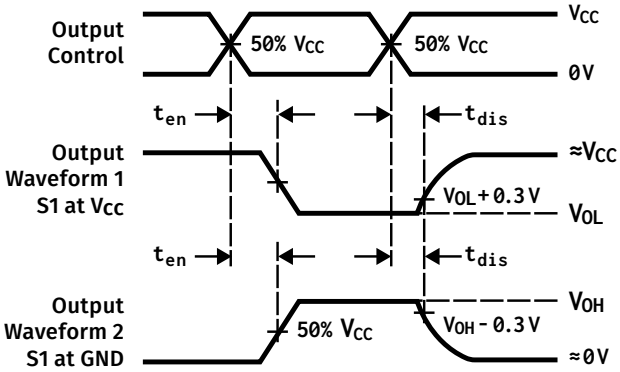


Figure 5: Enable and Disable Time Measurements

6 DETAILED DESCRIPTION

The AP54RHC505 is a 5-channel level translator with 3-state outputs and bus-keepers designed to operate from a wide supply voltage of 1.65 to 5.5 V with fully redundant input and output stages, providing for superior radiation resilience.

The output and input stages are constructed with transient-activated clamps (Figure 6, 7) that prevent inadvertent biasing of the V_{CC} power rail through parasitic diodes inherent to conventional input, output, and ESD circuits. The IC also incorporates an internal power-on reset (POR) circuit guaranteeing correct operation at power supply voltages as low as 1.65 V.

The bus-keeper functionality applies to all inputs and outputs when device is powered up above POR threshold. The buskeeper will hold the inputs or tri-stated outputs in their current logic state unless over-driven with a current greater than the bus-keep over drive current (Ibo).

The AP54RHC family's I/O protection circuitry allows for cold sparing configurations as it avoids a leakage current penalty on inputs and outputs while in a power-down state. This can result in considerable power savings in systems where multiple-path redundancy is employed. The ESD clamp circuits for this logic family are designed to support Class 2 ESD levels of 4 kV HBM and 500 V CDM.

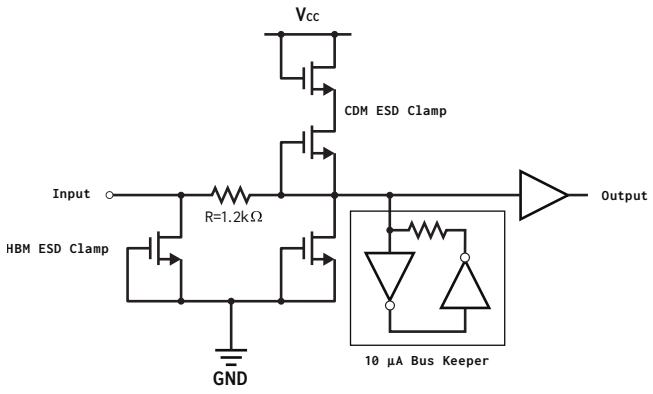


Figure 6: Input Pin Structure

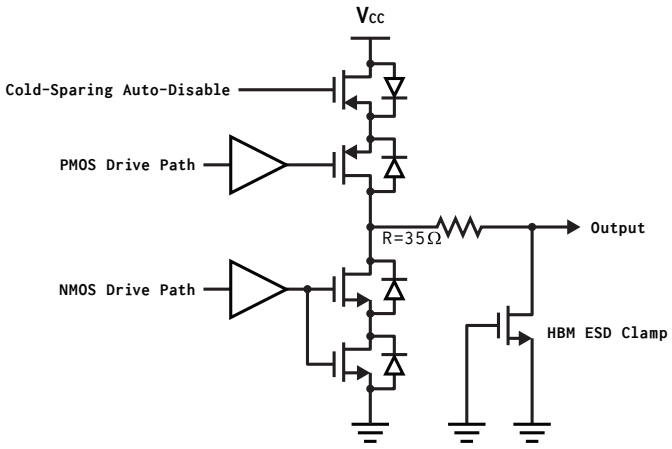


Figure 7: Output Pin Structure

7 APPLICATIONS INFORMATION

The AP54RHC505 provides a simple and robust means of interfacing digital logic between different voltage levels and domains. It can shift logic signals up from a lower voltage to a higher voltage or shift signals down from higher to lower voltages.

As seen in Table 1, the AP54RHC505 offers several features that make interfacing between different domains simple. First, the absence of an input supply voltage results in a tri-state condition at the output. Second, the outputs may also be tri-stated through assertion of the $\overline{OE}$ pin, which can be tied with power-supply enables or other control signals.

With the bus keeping feature on all inputs and outputs, the AP54RHC505 is capable of maintaining an output state even if an input is left floating. For example, this may be as a result of an input being connected to a tri-state output that has been placed in the tri-state mode after asserting the logic level of interest. In this scenario, the AP54RHC505 will not change the input voltage, nor the output state unless the level being asserted at the input is accompanied by a current driving capability beyond that of the bus keeper. Additionally, when the outputs are in tri-state the output buskeeper will hold the outputs at their current logic state, unless externally driven greater than capability of the bus keeper. When the power supplies are below the POR threshold, all bus keep circuits are disabled allowing for a cold spare configuration.

In an application utilizing a modern FPGA with 1.8 V I/O buffers that needs to interface to systems running at higher voltages (i.e. 5 V), the AP54RHC505 can be used to shift these signals to a range appropriate for the FPGA. The AP54RHC505 provides integrated triple modular redundancy (TMR), as well as SET resiliency on each buffer. In the event the 5 V supply is off, the AP54RHC505 will automaticaly tri-state the output buffers. The $\overline{OE}$ pin of the device can be tied to the FPGA power-enable logic such that $\overline{OE}$ is de-asserted when the 1.8 V I/O rail is not present.

7.1 APPLICATIONS EXAMPLE

As the AP54RHC family is radiation-hardened by design and includes internal TMR, it can be utilized in high-reliablity applications without additional supporting circuitry or devices. Nonetheless, some application requirements call for fully-redundant designs, where an “A” and a “B” device are required, often on separate power rails.

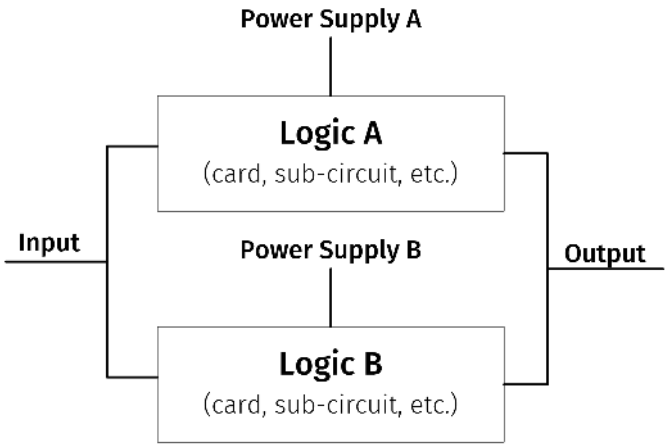


Figure 8: Two-Path Cold-Sparing Configuration

With the cold sparing capability of the AP54RHC family, fully redundant “A” and “B” functions may be placed in parallel (as seen in Figure 8) running off redundant power supplies. The inputs and outputs on each one of these functions are assumed to be based on the AP54RHC family, allowing for direct parallel connection without unwanted leakage current paths during cold sparing. In the event of a failure in power supply A or within function

A, the system can simply shut power supply A off and switch on power supply B, without requiring additional input or output switching or configuration changes.

7.2 POWER SUPPLY RECOMMENDATIONS

This device can operate at any voltage within the range specified in Table 4 Recommended Operating Conditions.

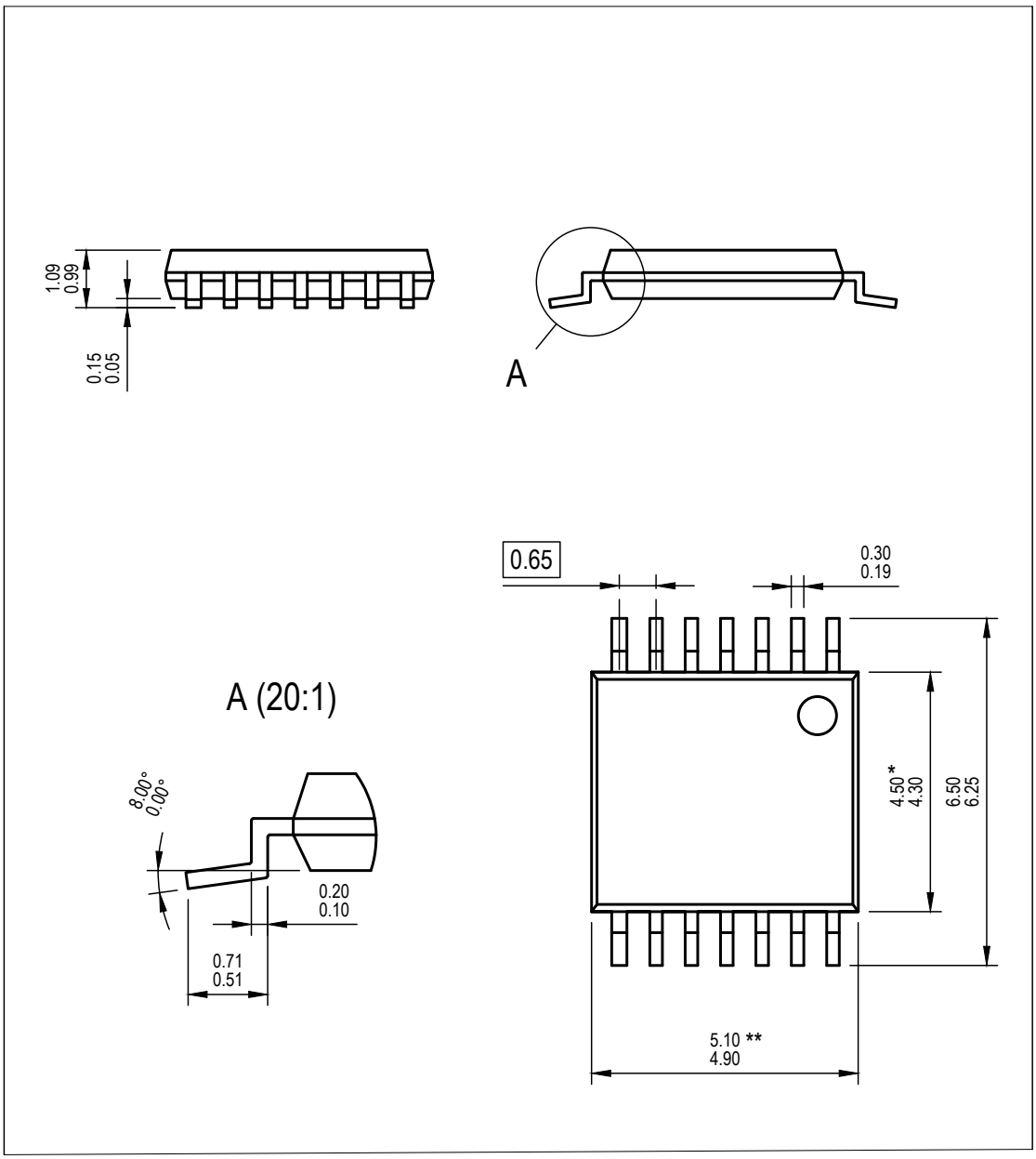
At a minimum, a 16 VDC (or higher), X7R-rated 0.1 µF ceramic decoupling capacitor should be placed near (within 1 cm) the V_{CC} pins of the device.

7.3 APPLICATION TIPS

Unused inputs of the level translator may be left floating, due to the internal bus-keeping feature. However, the output state of the device is undefined if the inputs are left floating when powering up the device — a valid logic level must be asserted at each input for the bus keeper to capture its state.

An unused **output** may be left unconnected. However, if the output is held in tristate, it is recommended to weakly bias the output to a valid logic level to prevent increased supply current. It is suggested that it be routed to a test point or similar accessible structure in case the associated function needs to be utilized as part of a design revision.

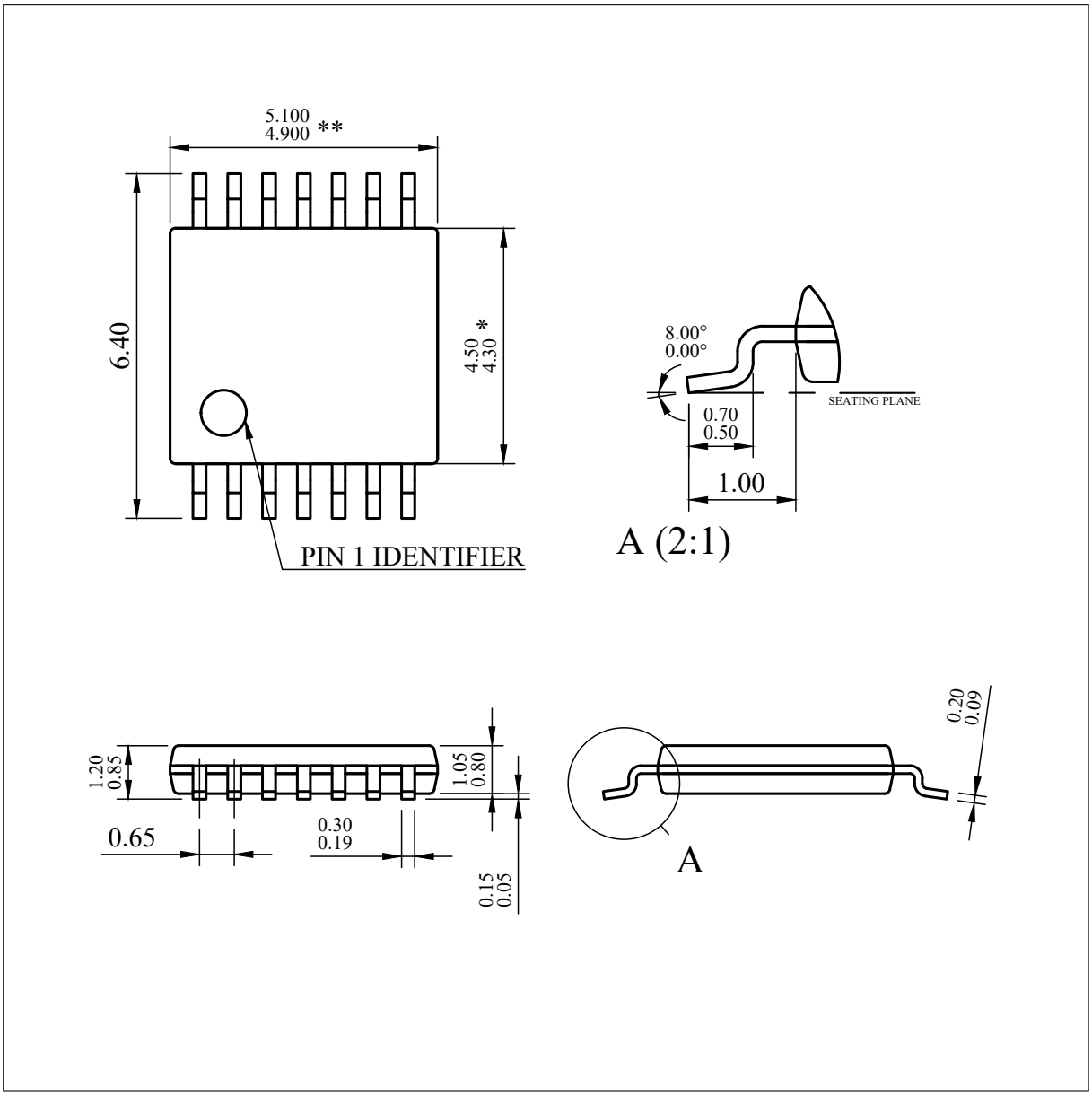
8 PACKAGING INFORMATION



Notes:
1. All linear dimensions are in millimeters. Dimensioning and tolerancing are as per ISO/TS 128-71:2010
2. The part is compliant with JEDEC MO-153 specifications.

* Body width does **not** include interlead flash. Interlead flash shall not exceed 0.25 mm each side.
** Body length does **not** include mold flash, protrusion, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0.15 mm on each side.

Figure 9: 14-LT - Package Mechanical Drawing (SnPb)



Notes:
1. All linear dimensions are in millimeters. Dimensioning and tolerancing are as per ISO/TS 128-71:2010
2. The part is compliant with JEDEC MO-153 specifications.

* Body width does **not** include interlead flash. Interlead flash shall not exceed 0.25 mm each side.
** Body length does **not** include mold flash, protrusion, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0.15 mm on each side.

Figure 10: 14-NT - Package Mechanical Drawing (NiPdAu)

9 ORDERING INFORMATION

Example part numbers for the AP54RHC505 are listed in Table 10. The full list of options for this part can be found in Figure 11. For a detailed description of product grades, please refer to Product Grades and Quality Flows document. Please contact Apogee Semiconductor sales at sales@apogeesemi.com for further information on sampling, lead time and purchasing on specific part numbers.

Table 10: AP54RHC505 Ordering Information

DEVICE	DESCRIPTION	PACKAGE	LEAD FINISH	PACKAGE DIAGRAM	PACKAGE MASS
AP54RHC505ALT-R	Rad-Hard 5-Channel Level Translator (30 krad (Si))	TSSOP-14	SnPb	14-LT	47 mg
AP54RHC505ALT-J(1)	Rad-Hard 5-Channel Level Translator (30 krad (Si))	TSSOP-14	SnPb	14-LT	47 mg
AP54RHC505BLT-R	Rad-Hard 5-Channel Level Translator (30 krad (Si))	TSSOP-14	SnPb	14-LT	47 mg
AP54RHC505BLT-J(1)	Rad-Hard 5-Channel Level Translator (30 krad (Si))	TSSOP-14	SnPb	14-LT	47 mg
AP54RHC505CLT-R	Rad-Hard 5-Channel Level Translator (30 krad (Si))	TSSOP-14	SnPb	14-LT	47 mg
AP54RHC505CLT-J(1)	Rad-Hard 5-Channel Level Translator (30 krad (Si))	TSSOP-14	SnPb	14-LT	47 mg
AP54RHC505ELT-R	Rad-Hard 5-Channel Level Translator (for eval only)	TSSOP-14	SnPb	14-LT	47 mg
AP54RHC505ELT-J(1)	Rad-Hard 5-Channel Level Translator (for eval only)	TSSOP-14	SnPb	14-LT	47 mg
AP54RHC505ANT-R	Rad-Hard 5-Channel Level Translator (30 krad (Si))	TSSOP-14	NiPdAu	14-NT	58 mg
AP54RHC505ANT-J(1)	Rad-Hard 5-Channel Level Translator (30 krad (Si))	TSSOP-14	NiPdAu	14-NT	58 mg
AP54RHC505BNT-R	Rad-Hard 5-Channel Level Translator (30 krad (Si))	TSSOP-14	NiPdAu	14-NT	58 mg
AP54RHC505BNT-J(1)	Rad-Hard 5-Channel Level Translator (30 krad (Si))	TSSOP-14	NiPdAu	14-NT	58 mg
AP54RHC505CNT-R	Rad-Hard 5-Channel Level Translator (30 krad (Si))	TSSOP-14	NiPdAu	14-NT	58 mg
AP54RHC505CNT-J(1)	Rad-Hard 5-Channel Level Translator (30 krad (Si))	TSSOP-14	NiPdAu	14-NT	58 mg
AP54RHC505ENT-R	Rad-Hard 5-Channel Level Translator (for eval only)	TSSOP-14	NiPdAu	14-NT	58 mg
AP54RHC505ENT-J(1)	Rad-Hard 5-Channel Level Translator (for eval only)	TSSOP-14	NiPdAu	14-NT	58 mg

(1) Available through distributors only.

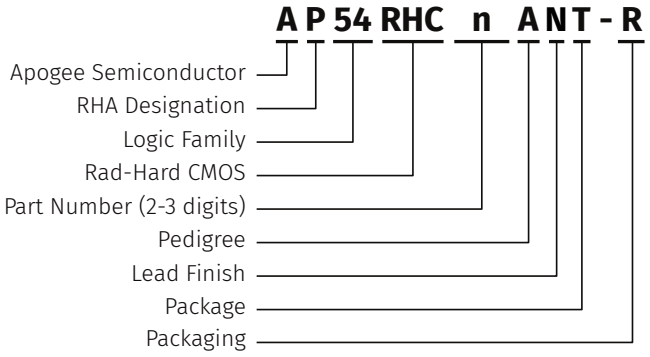


Figure 11: Part Number Decoder

1. RHA Designation
   - **P** 30 krad (Si)
   - **F** 300 krad (Si)
2. Part Number
   - **_** 505 (5-Channel Level Translator)
3. Pedigree
   - **A** -55 to +125 °C (Burn-in)
   - **B** -55 to +125 °C (No burn-in)
   - **C** 25 °C (No burn-in)
   - **E** 25 °C Functional Test Only (Evaluation)
4. Lead Finish
   - **L** Tin-Lead (SnPb)
   - **N** Nickel-Palladium-Gold (NiPdAu)
5. Package
   - **T** 14-pin Thin Shrink Small Outline Package (TSSOP)
6. Packaging
   - **R** Tape and Reel[1]
   - **J** JEDEC Tray

[1] Contact us for custom reel quantities. Orders less than full reel quantities may be shipped as cut tape.

10 REVISION HISTORY

REVISION	DESCRIPTION	DATE
B01	Updated logic diagram. Fixed typo in table 6 regarding I_{OZ} test conditions and bus-hold current. Updated detailed description. Updated ordering information.	2025-08-20
B00	Added $V_{CC}A/V_{CC}Y$ delay combinations to AC electrical characteristics (Table 7). Added bus keep table. Updated static characteristics. (Table 6). Renamed $\overline{EN}$ (enabled) pin to $\overline{OE}$ (output enabled). Added NiPdAu packaging option. Added package mass. Updated description.	2024-09-10
A05	Correct output pin structure diagram.	2021-12-06
A04	Updated ordering information.	2021-07-30
A03	Updated Static and Dynamic characteristics from test data.	2021-06-23
A02	Update Static and Dynamic characteristics.	2020-08-07
A01	Initial public release.	2020-02-29
A00	Initial internal release.	2019-07-05

For the latest version of this document, please visit https://www.apogeesemi.com.

11 LEGAL

All product, product specifications and data are subject to change without notice.

Apogee Semiconductor provides technical data (such as datasheets), design resources (including reference designs), reliability data (including performance in radiation environments), application or other design advice, safety information, and other resources **"as is"** and with all faults, and disclaims all warranties, express and implied, including without limitation any implied warranties of merchantability, fitness for a particular purpose or non-infringement of third party intellectual property rights. These resources are intended for skilled engineers with understanding of high reliability and high radiation environments and its complexities.

Apogee Semiconductor is not responsible for: (1) selecting the suitable products for a given application, (2) designing, verifying, validating and testing it, or (3) ensuring that it meets any performance, safety, security, or other requirements. These resources are subject to change without advance notice. The use of these resources is restricted to the development of an application that uses the Apogee Semiconductor products described in them. Other reproduction and display of these resources is prohibited. No license is granted to any other Apogee Semiconductor intellectual property right or to any third-party intellectual property right.

Apogee Semiconductor disclaims responsibility and reserves the right to demand indemnification for any claims, damages, costs, losses, and liabilities arising out of wrongful use of these resources. The products are provided subject to Apogee Semiconductor's Terms of Sale (https://www.apogeesemi.com/terms) or other applicable terms provided in conjunction with applicable products. The provision of these resources does not expand or otherwise alter applicable warranties or warranty disclaimers for Apogee Semiconductor products.

Purchasers of these products acknowledge that they may be subject to and agree to abide by the United States laws and regulations controlling the export of technical data, computer software, electronic hardware and other commodities. The transfer of such items may require a license from the cognizant agency of the U.S. Government.