Radiation Hardened level translating I²C, SMBUS, SPI I/O expander

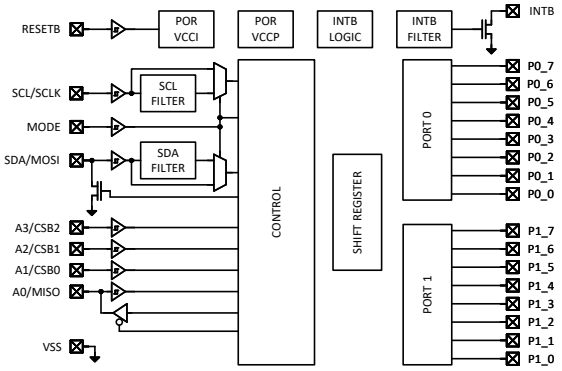
1 GENERAL DESCRIPTION

The **APIO16** is a radiation-hardened by design **level translating I²C, SMBUS, SPI I/O expander** that is ideally suited for space, medical imaging and other applications demanding radiation tolerance and high reliability. It is fabricated in a BiCMOS process utilizing proprietary radiation-hardening techniques, delivering high resiliency to single-event effects (SEE) and to a total ionizing dose (TID) as might be found in a Low Earth Orbit (LEO) environment.

Class 2 ESD protection on all inputs and outputs.

The APIO16 features extensive circuit techniques throughout, including triple modular redundancy, self correcting digital circuits and Dual Interlocked storage CEll (DICE) latches to ensure a high level of immunity to single-event transients (SET) and single event upset (SEU) without requiring additional redundant devices.

For more demanding radiation tolerance, see Geosynchronous Earth Orbit (GEO) version **AFIO16**



1.1 FEATURES

- 16-bit general purpose I/O expander
- MODE pin selects between SPI and I²C / SMBUS operation
- I²C: 16 addresses, pin configurable: allows up to 16 APIO16 devices to share the same I²C bus
- SPI mode has 3 Chip select pins allowing built in address decoding
- **1.4 VDC to 5.5 VDC** operation
- Extended operating temperature range (-55 °C to +125 °C)
- Package: 28pin TSSOP
- Open drain INTB pin to alert controller when inputs change
- Level translation, seperate power pins for I/O ports and serial interface
- Schmitt trigger on all port inputs
- Schmitt trigger on serial interface inputs and filter when in I²C mode
- **1 MHz Fast mode plus I²C, 25 MHz SPI**
- Input/Output Configuration register
- Polarity Inversion register
- Internal power-on reset, no glitch on power-up
- Cold spareable I/Os
- Latched outputs with **21mA** sink and source drive
- **Built-in triple redundancy** for enhanced reliability
- Class 2 ESD protection (4000 V HBM, 500 V CDM)
- TID resilience: **56 krad (Si)**
- SEL/SEU/SEFI resilience: LET of **77 MeV-cm²/mg**

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2 ACRONYMS AND ABBREVIATIONS

ESD	Electrostatic Discharge
RHA	Radiation Hardness Assurance
SEFI	Single Event Functional Interrupt
SET	Single Event Transient
TMR	Triple Modular Redundancy
HBM	Human-body Model
POR	Power On Reset
SEE	Single Event Effects
SEL	Single Event Latchup
TID	Total Ionizing Dose
CDM	Charged-device Model

3 PIN CONFIGURATION

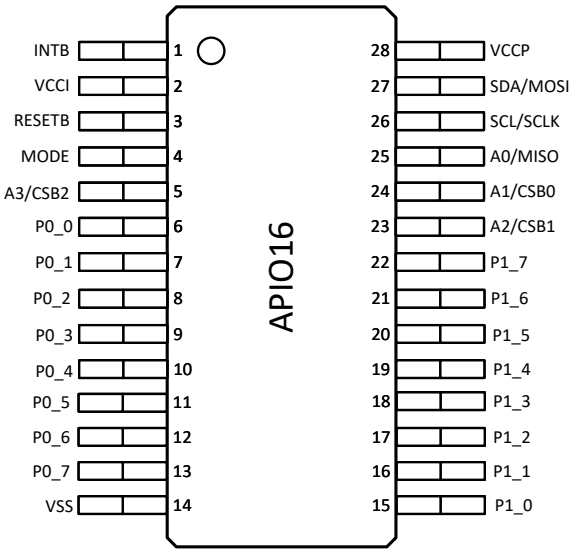


Table 1: APIO16 device pinout description

PIN NAME(S)	PIN NUMBER(S)	DESCRIPTION	
		MODE=low (I^2C)	MODE=hi (SPI)
SCL/SCLK	26	I^2C SCL	SPI SCLK input
SDA/MOSI	27	I^2C SDA	SPI MOSI input
A3/CSB2	5	address bit A3	active low chip select CSB2
A2/CSB1	23	address bit A2	active low chip select CSB1
A1/CSB0	24	address bit A1	active low chip select CSB0
A0/MISO	25	address bit A0	MISO tri-state output
INTB	1	open drain active low interrupt output, pull up to a 5.5V maximum rail through a pull-up resistor	
RESETB	3	active low reset input pull up to VCCI if not required	
MODE	4	if low, part operates with an I^2C interface, if high, part operates with an SPI interface. Tie to VSS or VCCI	
VCCI	2	supply voltage for all pins other than ports	
P0_0	6	port 0 input/output 0	
P0_1	7	port 0 input/output 1	
P0_2	8	port 0 input/output 2	
P0_3	9	port 0 input/output 3	
P0_4	10	port 0 input/output 4	
P0_5	11	port 0 input/output 5	
P0_6	12	port 0 input/output 6	
P0_7	13	port 0 input/output 7	
VSS	14	ground	
P1_0	15	port 1 input/output 0	
P1_1	16	port 1 input/output 1	
P1_2	17	port 1 input/output 2	
P1_3	18	port 1 input/output 3	
P1_4	19	port 1 input/output 4	
P1_5	20	port 1 input/output 5	
P1_6	21	port 1 input/output 6	
P1_7	22	port 1 input/output 7	
VCCP	28	supply voltage for ports	

4 ELECTRICAL CHARACTERISTICS

The sign convention for current follows JEDEC standards with negative values representing current sourced from the device and positive values representing current sunk into the device.

4.1 ABSOLUTE MAXIMUM RATINGS

Excursions beyond the values listed in Table 2 may cause permanent damage to the device. Proper function of the device cannot be guaranteed if these values are exceeded, and long-term device reliability may be affected. Functionality of the device at these values, or beyond those listed in Recommended Operating Conditions (Table 3) is not guaranteed.

All parameters are specified across the entire operating temperature range unless otherwise specified.

Table 2: Absolute Maximum Ratings

SYMBOL	PARAMETER		VALUE	UNITS
V_{CCI}, V_{CCP}	Supply voltage		-0.3 to +5.5	V
V_I	INTB, RESETB, MODE, A3_CSB2,P0_1, P0_2, P0_3, P0_4, P0_5, P0_6, P0_7, P1_1, P1_2, P1_3, P1_4, P1_5, P1_6, P1_7, A2/CSB1, A1/CSB0, A0/MISO, SCL/SCLK, SDA/MOSI		-0.3 to +5.5	V
I_{IK}	maximum current into input pins		-100 to 100	mA
I_O	maximum current into output pins		-100 to 100	mA
I_{CCI}	maximum current into V_{CCI} pin		-100 to 100	mA
I_{CCP}	maximum current into V_{CCP} pin		-100 to 420	mA
I_{VSS}	maximum current out of VSS pin		-420 to 100	mA
V_{ESD}	ESD Voltage	HBM	> 4000	V
		CDM	> 500	V
T_J	Operating junction temperature range		-55 to +150	°C
T_{STG}	Storage temperature range		-65 to +150	°C

4.2 RECOMMENDED OPERATING CONDITIONS

All recommended parameters below are specified across the entire operating temperature range unless otherwise specified.

Table 3: Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	MAX	UNITS
V_{CCI}, V_{CCP}	supply voltages	1.4	5.5	V
V_I	INTB, RESETB, MODE, A3_CSB2,P0_1, P0_2, P0_3, P0_4, P0_5, P0_6, P0_7, P1_1, P1_2, P1_3, P1_4, P1_5, P1_6, P1_7, A2/CSB1, A1/CSB0, A0/MISO, SCL/SCLK, SDA/MOSI	0	5.5	V
V_{O_I}	output voltage on serial interface pins	0	V_{CCI}	V
V_{O_P}	output voltage on port pins	0	V_{CCP}	V
I_{OL}	LOW level output current on serial interface or port pins	-	25	mA
I_{OH}	HIGH level output current on serial interface or port pins	-	-25	mA
I_{CCP}	Current into VCCP pin	-	410	mA
I_{VSS}	Current out of VSS pin	-	-410	mA

Table 4: Thermal Information

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
T_J	Operating junction temperature	-55	-	+125	°C
$R_{\theta JA}$	Junction to ambient thermal resistance	-	70 TBD	-	°C/W

4.3 ELECTRICAL CHARACTERISTICS

All parameters are specified across the entire operating temperature range and entire recommended operating range unless otherwise specified.

Table 5: Electrical Characteristics: general

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CCI_START}	V_{CCI} POR start voltage		-	1.13	1.36	V
V_{CCP_START}	V_{CCP} POR start voltage		-	1.13	1.36	V
V_{CCI_STOP}	V_{CCI} POR stop voltage		0.8	1.08	-	V
V_{CCP_STOP}	V_{CCP} POR stop voltage		0.8	1.08	-	V
V_{CCI_HYST}	V_{CCI} POR hysteresis		25	52	110	mV
V_{CCP_HYST}	V_{CCP} POR hysteresis		25	52	110	mV
V_{IL_I}	SDA/MOSI, SCL/SCLK, A0, A1/CSB0, A2/CSB1, A3/CSB2, MODE, RESETB pin low level input voltage	V_{CCI} = 5.5V	1.65	2.43	2.7	V
		V_{CCI} = 3.0V	0.9	1.3	1.5	
		V_{CCI} = 1.65V	0.495	0.68	0.83	
		V_{CCI} = 1.4V, 0°C to 110°C	0.42	0.56	0.7	
V_{IH_I}	SDA/MOSI, SCL/SCLK, A0, A1/CSB0, A2/CSB1, A3/CSB2, MODE, RESETB pin high level input voltage	V_{CCI} = 5.5V	2.65	2.86	3.85	V
		V_{CCI} = 3.0V	1.45	1.62	2.1	
		V_{CCI} = 1.65V	0.84	0.97	1.15	
		V_{CCI} = 1.4V, 0°C to 110°C	0.75	0.85	0.98	
$V_{I\_HYS\_I}$	SDA/MOSI, SCL/SCLK, A0, A1/CSB0, A2/CSB1, A3/CSB2, MODE, RESETB pin input hysteresis	V_{CCI} = 5.5V	0.3	0.44	0.6	V
		V_{CCI} = 3.0V	0.22	0.32	0.46	
		V_{CCI} = 1.65V	0.15	0.29	0.45	
		V_{CCI} = 1.4V, 0°C to 110°C	0.15	0.29	0.4	
V_{IL_P}	port pin low level input voltage	V_{CCP} = 5.5V	1.65	2.43	2.7	V
		V_{CCP} = 3.0V	0.9	1.3	1.5	
		V_{CCP} = 1.65V	0.495	0.68	0.83	
		V_{CCP} = 1.4V, 0°C to 110°C	0.42	0.56	0.7	
V_{IH_P}	port pin high level input voltage	V_{CCP} = 5.5V	2.65	2.86	3.85	V
		V_{CCP} = 3.0V	1.45	1.62	2.1	
		V_{CCP} = 1.65V	0.84	0.97	1.15	
		V_{CCP} = 1.4V, 0°C to 110°C	0.75	0.85	0.98	
$V_{I\_HYS\_P}$	port pin input hysteresis	V_{CCP} = 5.5V	0.3	0.44	0.6	V
		V_{CCP} = 3.0V	0.22	0.32	0.46	
		V_{CCP} = 1.65V	0.15	0.29	0.45	
		V_{CCP} = 1.4V, 0°C to 110°C	0.15	0.29	0.4	

Table 6: Electrical Characteristics: general

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OH_P}	port pin output high voltage	V_{CCP} = 5.5V, I_{OH_P} = -25mA	4.9	5.0	-	V
		V_{CCP} = 3.0V, I_{OH_P} = -25mA	2.15	2.4	-	
		V_{CCP} = 5.5V, I_{OH_P} = -10mA	5.25	5.3	-	
		V_{CCP} = 3.0V, I_{OH_P} = -10mA	2.65	2.75	-	
		V_{CCP} = 1.65V, I_{OH_P} = -10mA	1.05	1.30	-	
		V_{CCP} = 1.4V, I_{OH_P} = -4mA, 0°C to 110°C	1.16	1.22	-	
V_{OL_P}	port pin output low voltage	V_{CCP} = 5.5V, I_{OL_P} = 25mA	-	0.32	0.45	V
		V_{CCP} = 3.0V, I_{OL_P} = 25mA	-	0.42	0.68	
		V_{CCP} = 5.5V, I_{OL_P} = 10mA	-	0.13	0.18	
		V_{CCP} = 3.0V, I_{OL_P} = 10mA	-	0.16	0.25	
		V_{CCP} = 1.65V, I_{OL_P} = 10mA	-	0.28	0.51	
		V_{CCP} = 1.4V, I_{OL_P} = 4mA, 0°C to 110°C	-	0.14	0.22	
V_{OH_I}	MISO pin output high voltage	V_{CCI} = 5.5V, I_{OH_I} = -25mA	4.9	5.0	-	V
		V_{CCI} = 3.0V, I_{OH_I} = -25mA	2.15	2.4	-	
		V_{CCI} = 5.5V, I_{OH_I} = -10mA	5.25	5.3	-	
		V_{CCI} = 3.0V, I_{OH_I} = -10mA	2.65	2.75	-	
		V_{CCI} = 1.65V, I_{OH_I} = -10mA	1.05	1.3	-	
		V_{CCI} = 1.4V, I_{OH_I} = -4mA, 0°C to 110°C	1.16	1.22	-	
V_{OL_I}	INTB, MISO, SDA pin output low voltage	V_{CCI} = 5.5V, I_{OL_I} = 25mA	-	0.32	0.45	V
		V_{CCI} = 3.0V, I_{OL_I} = 25mA	-	0.42	0.68	
		V_{CCI} = 5.5V, I_{OL_I} = 10mA	-	0.13	0.18	
		V_{CCI} = 3.0V, I_{OL_I} = 10mA	-	0.16	0.25	
		V_{CCI} = 1.65V, I_{OL_I} = 10mA	-	0.28	0.51	
		V_{CCI} = 1.4V, I_{OL_I} = 4mA, 0°C to 110°C	-	0.14	0.22	
I_{OH_P}	port pin output high current	V_{CCP} = 5.5V, V_{OH_P} = 5.1V	-	-21	-16	mA
		V_{CCP} = 3.0V, V_{OH_P} = 2.6V	-	-17	-12	
		V_{CCP} = 1.65V, V_{OH_P} = 1.25V	-	-11	-6	
		V_{CCP} = 1.4V, V_{OH_P} = 1V, 0°C to 110°C	-	-9	-4	
I_{OL_P}	port pin output low current	V_{CCP} = 5.5V, V_{OL_P} = 0.4V	22	31	-	mA
		V_{CCP} = 3.0V, V_{OL_P} = 0.4V	15	24	-	
		V_{CCP} = 1.65V, V_{OL_P} = 0.4V	7	13	-	
		V_{CCP} = 1.4V, V_{OL_P} = 0.4V, 0°C to 110°C	5	10	-	

Table 7: Electrical Characteristics: general

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{OH_I}	MISO pin output high current	V_{CCI} = 5.5V, V_{OH_I} = 5.1V	-	-21	-16	mA
		V_{CCI} = 3.0V, V_{OH_I} = 2.6V	-	-17	-12	
		V_{CCI} = 1.65V, V_{OH_I} = 1.25V	-	-11	-6	
		V_{CCI} = 1.4V, V_{OH_I} = 1V, 0°C to 110°C	-	-9	-4	
I_{OL_I}	INTB, MISO, SDA pin output low current	V_{CCI} = 5.5V, V_{OL_I} = 0.4V	25	50	-	mA
		V_{CCI} = 3.0V, V_{OL_I} = 0.4V	20	37	-	
		V_{CCI} = 1.65V, V_{OL_I} = 0.4V	8	19	-	
		V_{CCI} = 1.4V, V_{OL_I} = 0.4, 0°C to 110°C	6	14	-	
I_{VCCI_Q}	quiescent supply current into V_{CCI}	V_{CCI} = 5.5V, all ports inputs tied to VSS or 5.5V, no communications	-	220	300	uA
I_{VCCP_Q}	quiescent supply current into V_{CCP}	V_{CCP} = 5.5V, all ports inputs tied to VSS or 5.5V	-	30	50	uA
C_{IP}	port pin capacitance when port configured as input(1)		-	TBD	-	pF
t_{V_INTB}	Time from change on input port to INTB valid		500	-	1200	ns
t_{RESET_W}	required RESETB pulse width		200	-	-	ns
t_{RESET_R}	recovery from RESETB		200	-	-	ns
t_{RESET_A}	time for RESETB to affect ports	-	-	-	200	ns

(1) not tested in production

Table 8: Electrical Characteristics: I^2C/SMBUS operation

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_I	Input leakage on RESETB, A3,A2,A1,A0	V_I=5.5V or VSS	-1	-	1	uA
I_{OL_SDA}	I^2C SDA pin low level sink current	V_{SDA}=0.4V, V_{CCI}=3.0V	20	37	-	mA
I_{OL_SDA}	I^2C SDA pin low level sink current	V_{SDA}=0.4V, V_{CCI}=1.65V	8	19	-	mA
I_{OL_SDA}	I^2C SDA pin low level sink current	V_{SDA}=0.4V, V_{CCI}=1.4V, 0°C to 110°C	6	14	-	mA
C_I	SCL, SDA input capacitance(1)		-	TBD	TBD	pF
f_{SCL}	SCL clock frequency	V_{CCI}=3.0	-	-	1000	kHz
f_{SCL}	SCL clock frequency	V_{CCI}=1.65V	-	-	400	kHz
f_{SCL}	SCL clock frequency	V_{CCI}=1.4V, 0°C to 110°C	-	-	100	kHz
t_{SCH}	SCL high time		260	-	-	ns
t_{SCL}	SCL low time		500	-	-	ns
t_{SP}	SCL, SDA maximum width of spike suppressed by input filter		50	-	200	ns
t_{SDS_I2C}	Data setup time	V_{CCI}=3.0	50	-	-	ns
t_{SDS_I2C}	Data setup time	V_{CCI}=1.65	100	-	-	ns
t_{SDS_I2C}	Data setup time	V_{CCI}=1.4V, 0°C to 110°C	250	-	-	ns
t_{SDH_I2C}	Data hold time		0	-	-	ns
t_{ICR_I2C}	Input rise time		-	-	120	ns
t_{ICF_I2C}	Input fall time		-	-	120	ns
t_{OCF_I2C}	Output fall time		-	-	TBD	ns
t_{BUF}	Bus free time between stop and start		-	-	500	ns
t_{STS}	Start or repeated start setup time		-	-	260	ns
t_{STH}	Start or repeated start hold time		-	-	260	ns
t_{SPS}	Stop setup time		-	-	260	ns
t_{VD}	SCL low to valid data		-	-	450	ns
t_{VDACK}	SCL low to valid ACK		-	-	450	ns
$t_{RST\_INTB\_I2C}$	Read of input port to INTB valid		500	-	1200	ns
t_{VQ_I2C}	Write of output port to port valid		70	-	200	ns
t_{SUDP_I2C}	Setup data on port before read		TBD	-	TBD	ns
t_{HDP_I2C}	Hold data on port after read		TBD	-	TBD	ns

(1) not tested in production

Table 9: Electrical Characteristics: SPI operation

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
f_{SCLK}	SCLK clock frequency	V_{CCI}= 3.0V	-	-	25	MHz
f_{SCLK}	SCLK clock frequency	V_{CCI} = 1.65V	-	-	10	MHz
f_{SCLK}	SCLK clock frequency	V_{CCI}=1.4V, 0°C to 110°C	-	-	2	MHz
t_{HIGH}	clock high time		TBD15	-	-	ns
t_{LOW}	clock low time		TBD15	-	-	ns
t_{SU_CSB}	CSBx setup time before first SCLK rising edge		TBD50	-	-	ns
t_{H_CSB}	CSBx hold time after last SCLK falling edge		TBD50	-	-	ns
$t_{SU\_DAT\_SPI}$	data setup time for SPI interface		TBD50	-	-	ns
$t_{HD\_DAT\_SPI}$	data hold time for SPI interface		0	-	-	ns
$t_{RST\_INTB\_SPI}$	Time from read of input port to INTB valid		TBD500	-	TBD1000	ns
$t_{V\_Q\_SPI}$	Time from write of output port to port valid		TBD	-	TBD	ns
$t_{SU\_DP\_SPI}$	setup time for data on port before read from port		TBD	-	TBD	ns
$t_{H\_DP\_SPI}$	hold time for data on port after read from port		TBD	-	TBD	ns
t_{VD_SPI}	time from falling edge of SCLK to valid data on MISO	V_{CCI} = 3.0V	TBD	-	TBD	ns
t_{VD_SPI}	time from falling edge of SCLK to valid data on MISO	V_{CCI} = 1.65V	TBD	-	TBD	ns
t_{VD_SPI}	time from falling edge of SCLK to valid data on MISO	V_{CCI}=1.4V, 0°C to 110°C	TBD	-	TBD	ns
t_{DIS_MOSI}	time from CSBx rising to high impedance on MISO	V_{CCI} = 3.0V	5	-	30	ns
t_{DIS_MOSI}	time from CSBx rising to high impedance on MISO	V_{CCI} = 1.65V	-	-	40	ns
t_{DIS_MOSI}	time from CSBx rising to high impedance on MISO	V_{CCI}=1.4V, 0°C to 110°C	-	-	50	ns

5 TYPICAL CHARACTERISTICS

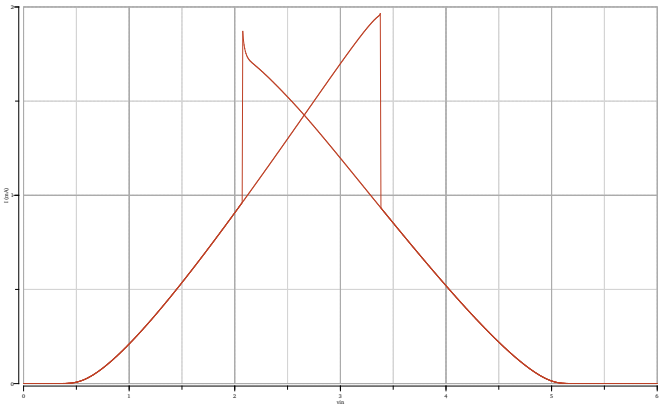
Include following typical curves here:

I_{VCCI_Q} Quiescent supply current into VCCI versus temperature

I_{VCCP_Q} Quiescent supply current into VCCP versus temperature

V_{CCP}- V_{OH_P} High level output voltage on port pin versus temperature

V_{OL_P} Low level output voltage on port pin versus temperature



Increase in I_{VCCP_Q} from single port pin swept from 0V to 5.5V with V_{CCI} = 5.5V (typical 27C)

6 DETAILED DESCRIPTION

The APIO16 is a level translating I^{2}C, SMBUS, SPI I/O expander. Please refer to the block diagram in Figure 2. The device incorporates a bi-directional serial bus and two 8-bit ports which can be controlled by and inspected by an external controller on the bus. The device can support two different types of serial bus: I^{2}C and SPI bus. The type of bus used is set by tying the MODE pin to either VSS or VCCI. Each pin on each port can be individually programmed to be enabled as an output or disabled. When enabled as an output, the pin can drive high or low. At any time, the logic state on the pin can be read back via the serial interface. When the pins on the port are read, the state of the pins is saved in an internal register. If any of the pins configured as inputs changes from the value saved in the internal register, the INTB pin is pulled low, to alert the controller that the inputs have changed from the values last read on that port. Each of these functions is explained in more detail in the following sections.

6.1 FUNCTIONAL BLOCK DIAGRAM

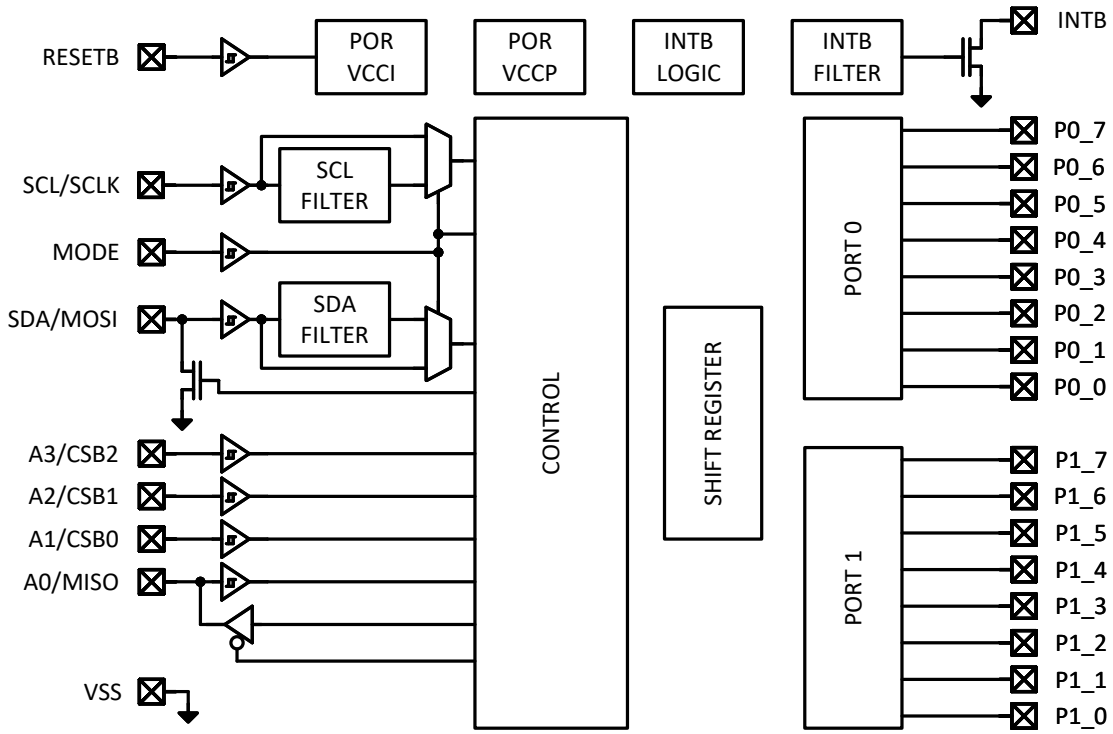


Figure 1: block diagram

6.2 POR VCCI

The device serial interface is powered through the VCCI pin.

There is a Power On Reset (POR) circuit which monitors the VCCI supply. If VCCI drops below $\mathbf{V_{CCI\_STOP}}$ all internal registers are reset to initial conditions. The ports are reset to inputs only. The device cannot be programmed until VCCI is raised above $\mathbf{V_{CCI\_START}}$ and RESETB is high.

The APIO16 posesses proprietary cold sparing circuitry on all inputs and outputs, for both the port pins and the serial interface pins. If the VCCI POR detects a low supply voltage on VCCI, all inputs and outputs become high impedance and can be driven by other devices connected to the same pins without exhibiting leakage. This allows the device to be used to construct "Cold Spareable" systems.

6.3 RESETB

If the RESETB pin is pulled low, the serial interface is cleared, all internal registers are reset to initial conditions. The ports are reset to inputs only. The effect is identical to POR VCCI. If the POR VCCI has already been released by VCCI raising above $\mathbf{V_{CCI\_START}}$ then the device will be capable of being programmed as soon as RESETB is raised to a high level, otherwise the device will wait until VCCI has been raised above $\mathbf{V_{CCI\_START}}$. If RESETB functionality is not desired, tie the RESETB pin to VCCI.

6.4 POR VCCP

The device ports are powered through the VCCP pin. There is a Power On Reset (POR) circuit which monitors the VCCP supply. If VCCP drops below $\mathbf{V_{CCP\_STOP}}$ the ports go high impedance and are suitable for cold-sparing applications. In this condition, the serial interface sees all the inputs as being in the low state. If the ports have previously been read and previously had a different state to all pins being low, this will cause INTB to be pulled low (see section on INTB operation). If the ports are read, they will read as being "all low".

The VCCP POR being asserted does NOT clear the internal state of the serial interface to its power on reset condition, this means that once the VCCP is restored to a voltage above $\mathbf{V_{CCP\_START}}$, the ports assume the states controlled by the serial interface state. Consequently the APIO16 can be configured even with the VCCP supply pulled low, but the ports are not active until VCCP is raised.

6.5 MODE

The MODE pin controls whether the part functions with an I^2C interface (MODE pulled low) or an SPI interface (MODE pulled high). The MODE pin is not latched in the IC. It is recommended that the MODE pin be tied high (to VCCI) or low (to VSS), so that its state is stable when the IC powers up and is released from RESETB and it is recommended that the MODE pin is not changed during operation.

6.6 PORTS

There are two 8-bit ports: Port 0 and Port 1. All of the pins in an individual port can be configured, read or written at the same time. The power supply for the ports is VCCP, which is independent of the power supply for the serial interface: VCCI.

Within each port, each bit can be configured to be tri-state or driven and can be configured to drive high or low. In addition, the voltage on each port pin is converted to a logic value by a schmitt trigger. The resultant logic signal can be optionally inverted and the result can be read back by the controller. When driving the pin high, the pin is driven to the VCCP voltage. If the pin is configured to be tri-state, it can be driven externally to a voltage higher than the VCCP voltage up to the ABS MAX voltage of 5.5V without forward biasing any protection diodes and with no damage. If VCCP or VCCI are below their POR threshold, all port pins go into "high impedance" input state.

If the port pins are not lower than approximately 300mV above VSS or are not higher than approximately 300mV below VCCP, the internal Schmitt trigger circuits will cause some additional quiescent current to be drawn from the VCCP pin. Please see the typical characteristics plot of increase in $\mathbf{I_{VCC\_Q}}$ for a single port pin.

A simplified schematic of the circuitry within each port pin is shown in Figure 2

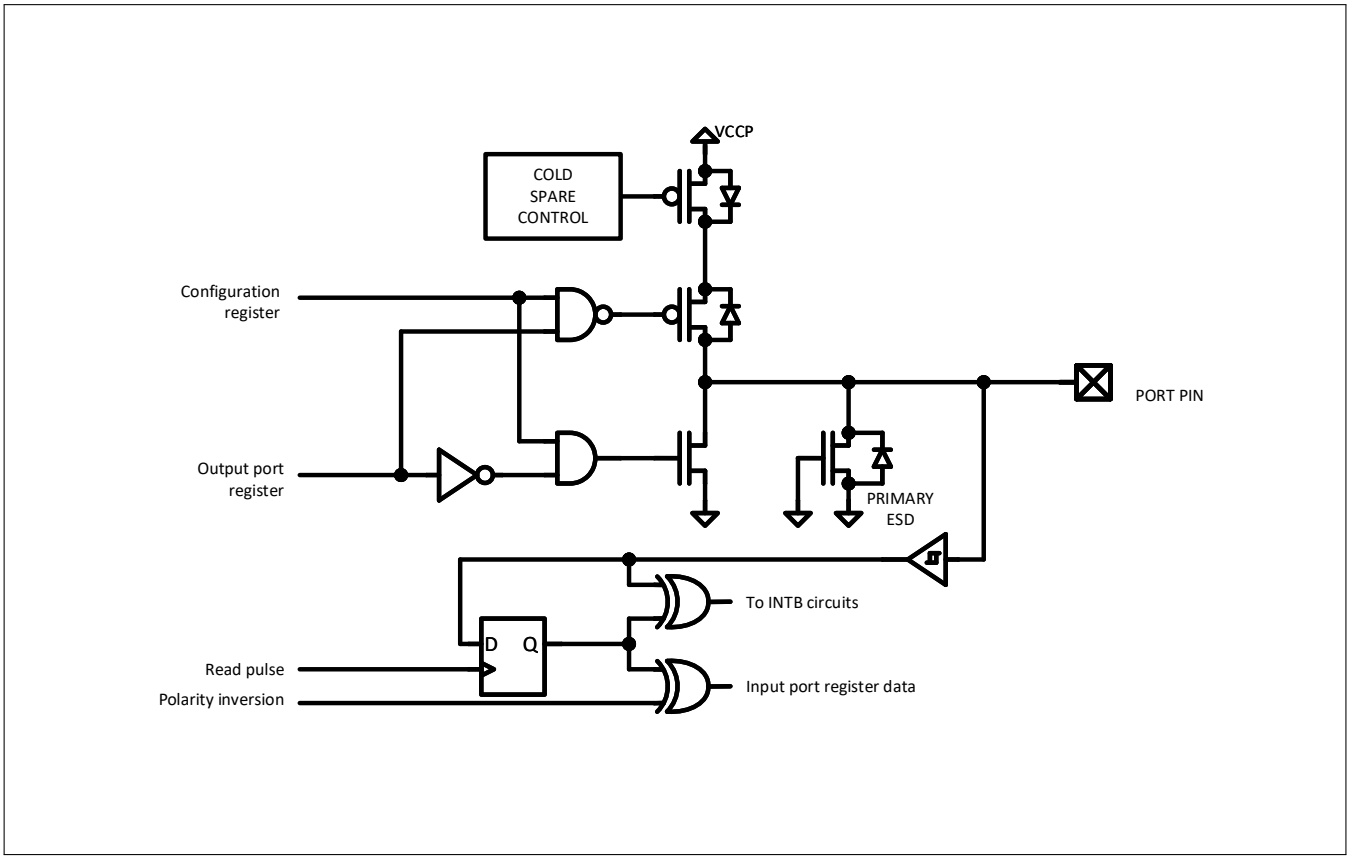


Figure 2: simplified port pin schematic

6.7 INTB

On a VCCI POR condition, or when RESETB is pulled low, the INTB pin goes high impedance, in addition two latches are cleared, indicating that neither port has been read since the last VCCI POR. When the ports are read, the current state of the port is stored in an internal register, in addition, the latch which stores whether the port has been read is set. The state of the pins on the port are continuously compared with the values in the register which stores the state of the inputs since the last read. If any of the inputs has a state different to the value last read AND the pin is configured to be an input AND the port that the input is a part of has been read since the last VCCI POR release, a signal is generated, which passes through a nominal 750ns filter. If the signal is present without changing for longer than the filter duration, the INTB pin will be pulled low, to indicate to the controller that one of the input pins has changed state.

If the changed pin goes back to its previous state OR the port that that pin is part of is read, the signal into the INTB filter is cleared. If it stays cleared for longer than the filter duration (750ns), then INTB will be set to a high impedance state again.

If the INTB pin functionality is not desired, it is recommended to tie INTB pin to VSS.

6.8 I^2C OPERATION

If the MODE pin is pulled low, the part operates in I^2C mode. In I^2C mode, the APIO16 is SMBUS 3.2 compliant. In I^2C operation the **APIO16** operates as a target device. There is an external device, typically a microcontroller or FPGA that acts as the controller. Communication is initiated by and controlled by the controller. There are two communications lines: SDA and SCL, which are typically pulled up by resistors. Multiple devices can be connected to the same SDA and SCL lines. There must be at least one controller in addition to the one or more

APIO16 devices, there may be other devices on the bus as well. Each target device on the bus has a device address. In the case of the **APIO16** , there is a range of 16 addresses that can be selected by hard wiring address pins. When the controller sends a command to a target device, it includes a target device address, to select which target device is to be addressed.

The SCL/SCLK pin functions as the SCL input pin in I^2C. The SCL FILTER is used to filter out glitches on the SCL line, it is guaranteed that glitches less than 50ns will be suppressed.

The SDA/MOSI pin functions as the SDA bidirectional pin in I^2C. The SDA FILTER is used to filter out glitches on the SDA line, it is guaranteed that glitches less than 50ns will be suppressed.

The A3/CSB2, A2/CSB1, A1/CSB0 and A0/MISO pins function as address pins A3, A2, A1 and A0 respectively. These pins select the I^2C address used by the device.

The seven bit I^2C device address selected by pulling the address pins high or low is listed in Table 10. Each I^2C command contains a 7-bit device address (dad[6:0]). If the address in the I^2C command matches the device address selected by the address pins on the device, the device will respond to the I^2C command. Otherwise, the device will ignore the command.

Table 10: APIO16 I^2C address

ADDRESS PINS				I^2C ADDRESS
A3	A2	A1	A0	(HEX)
L	L	L	L	20
L	L	L	H	21
L	L	H	L	22
L	L	H	H	23
L	H	L	L	24
L	H	L	H	25
L	H	H	L	26
L	H	H	H	27
H	L	L	L	28
H	L	L	H	29
H	L	H	L	2A
H	L	H	H	2B
H	H	L	L	2C
H	H	L	H	2D
H	H	H	L	2E
H	H	H	H	2F

6.8.1 I²C timing diagrams

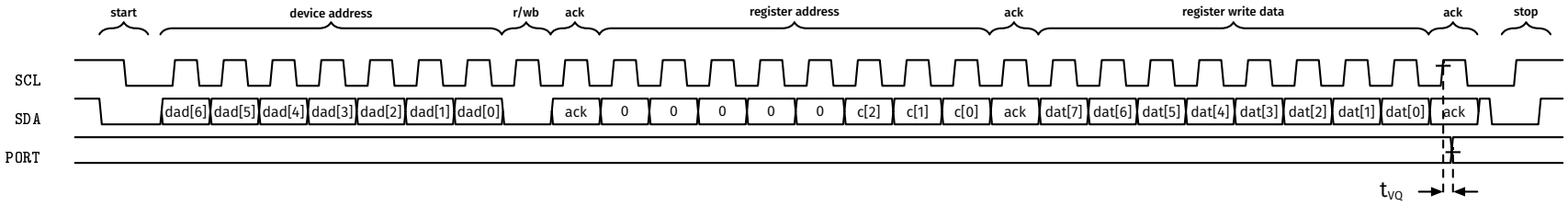


Figure 3: I²C timing diagram for single write operation

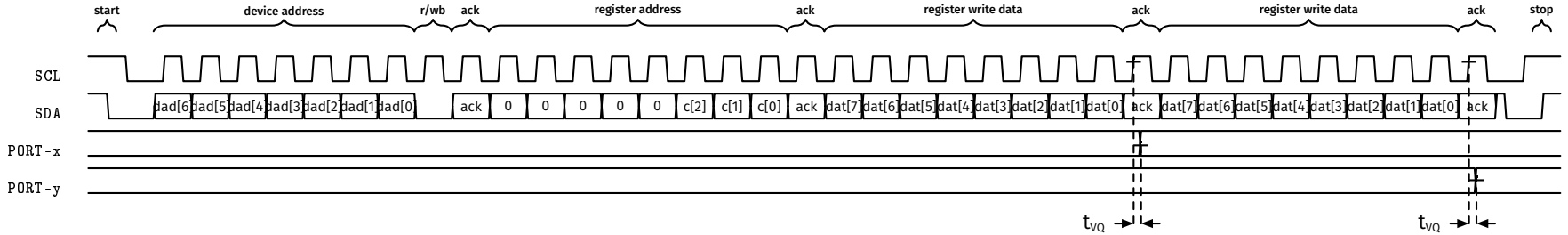


Figure 4: I²C timing diagram for two write operations

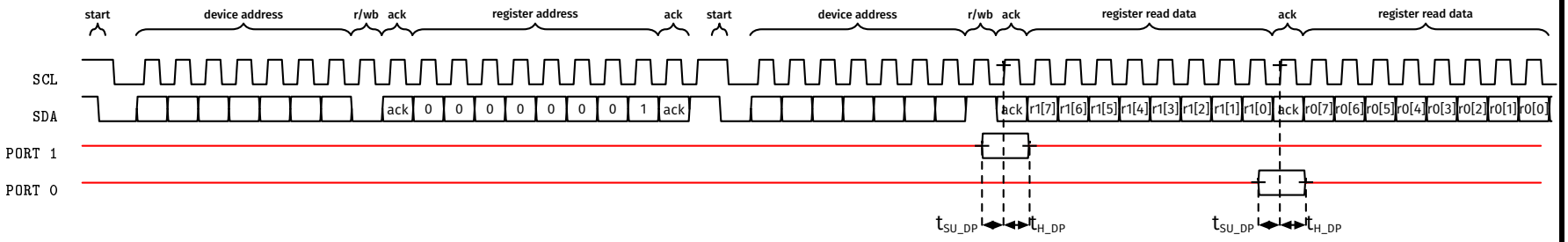


Figure 5: I²C port read timing specifications

Note: Red on PORT 0 and PORT 1 indicates "don't care"

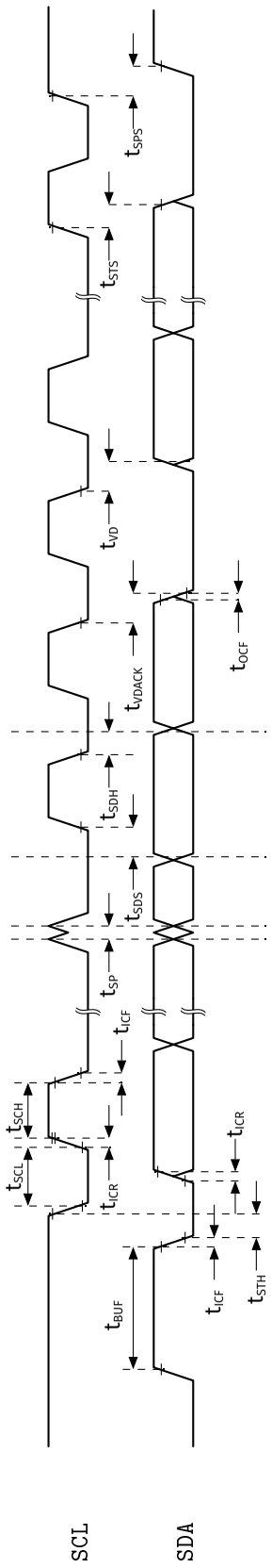


Figure 6: I²C timing specifications

6.8.2 I²C write

In Fig 3 we see the timing for a single write to the device. First, there is a START symbol followed by the target device address, sent MSB first (dad[6:0]) and then the r/wb bit, which will be low, indicating a write operation. Next, the target device acknowledges that it saw a correct address, pulling the SDA line low (ack). Next, the register address is sent, which tells the target which register to write to (rad[7:0]). rad[7:3] must all be zero, rad[2:0] are bits C2, C1, C0 as detailed in the REGISTER DESCRIPTIONS section. Next, the target acknowledges that it saw a valid command, pulling the SDA line low (ack). Next, the data to be written to the selected register is sent to the target (dat[7:0]), Next, the target acknowledges that it saw 8 bits of data, pulling the SDA line low (ack). Finally, there is a STOP symbol.

When a register is written in this manner, the register bits take effect after time: $\mathbf{t_{VQ}}$ after the rising edge of SCL during the final ack after the register data has been received.

In Fig 4 we see the timing for two consecutive writes to the device. First, there is a START symbol, followed by the target device address (dad[6:0]) and the r/wb bit, which will be low, indicating a write operation. Next, the target device acknowledges that it saw a correct address, pulling the SDA line low (ack). Next, the command word is sent, which tells the target which register to write to (rad[7:0]). rad[7:3] must all be zero, rad[2:0] are bits C2, C1, C0 as detailled in the REGISTER DESCRIPTIONS section. Next, the target acknowledges that it saw a valid command, pulling the SDA line low (ack). Next, the data to be written to the selected register is sent to the target (dat[7:0]), Next, the target acknowledges that it saw 8 bits of data, pulling the SDA line low (ack). Next, the data to be written to the next register is sent to the target (dat[7:0]), Next, the target acknowledges that it saw 8 bits of data, pulling the SDA line low (ack). Finally, there is a STOP marked in red.

When there are multiple I²C writes without start conditions between them, consecutive writes address the same type of register, but for the other port.

Examples:

If the first write addresses register 2, the second will address register 3, the third register 2, the fourth, register 3 and so on.

If the first write addresses register 3, the second will address register 2, the third register 3, the fourth, register 2 and so on.

If the first write addresses register 5, the second will address register 4, the third register 5, the fourth, register 4 and so on.

6.8.3 I²C read

The controller first must send the target **APIO16** address with r/wb bit sent to a logic "0" followed by the address of the register that it is desired to read. After the target ACK, the controller must send a repeated START condition (or a STOP followed by a START), followed by the target address once more and the r/wb bit set to a logic "1", the target will reply with an ACK. At this point, the controller must stop pulling SDA down , allowing the Target to send data back to the controller on the SDA line. As the SCL line is toggled by the controller, the target shifts out the read data, MSB first. At the end of the received byte, if the controller must provides an ACK to the target, the target will then provide another data word from the complimentary register as described in the below examples:

If the first register read is register 0, the second register read will be register 1, the third register 0, the fourth, register 1 and so on.

If the first register read is register 1, the second register read will be register 0, the third register 1, the fourth, register 0 and so on.

If the first register read is register 3, the second register read will be register 2, the third register 3, the fourth, register 2 and so on.

There is no limit to the number of reads that can be performed. To terminate reads, the controller must fail to provide an ACK to acknowledge the last data byte read.

Note: the polarity of the r/wb used in I^2C is the opposite to the polarity used in SPI

6.8.4 I^2C read from port

In I^2C mode, when reading from the port pins, the state of the port pins is latched shortly after the rising edge on SCL during the ACK just before the data is transferred from the target to the controller. To guarantee correctly latching the expected data on the pins, the data must be stable before and after that time, as shown in Figure 5

6.9 SPI OPERATION

If the MODE pin is pulled high, the part operates in SPI mode. In SPI operation the **APIO16** operates as a target device. There is an external device, typically a microcontroller or FPGA that acts as the Controller. Communication is initiated by and controlled by the controller. There are two communications lines from Controller to Target device: MOSI and SCLK. Multiple devices can be connected to the same MOSI and SCLK lines. There must be at least one controller in addition to the one or more **APIO16** devices, there may be other devices on the bus as well. The SDA/MOSI pin functions as the MOSI data from controller to target input pin. There is no deglitching of signals on MOSI in SPI mode. The SCL/SCLK pin functions as the SCLK clock input pin in SPI. There is no deglitching of signals on SCLK in SPI mode.

Each target **APIO16** device on the bus is selected by the CSB0, CSB1, CSB2 lines. The A3/CSB2, A2/CSB1, and A1/CSB0 pins function as CSB2, CSB1 and CSB0 respectively. The IC will ignore data on MOSI unless all three of CSB0, CSB1 and CSB2 are low. CSBx is used in the following sections to represent the boolean logical function: CSBx = (CSB0 OR CSB1 OR CSB2), the statement: "CSBx is low" will be taken to mean that all three of CSB0, CSB1 AND CSB2 are low simultaneously.

The A0/MISO pin functions as the tri-state output driver from the target to the controller. It is tri-state except when sending data back from target to controller.

Provided the VCCI is 3V or higher, the **APIO16** can support a maximum bus speed of 25MHz, provided all the timings required are met. Below 3V on VCCI, the **APIO16** can support a maximum bus speed of TBD 10 MHz.

6.9.1 SPI timing diagrams

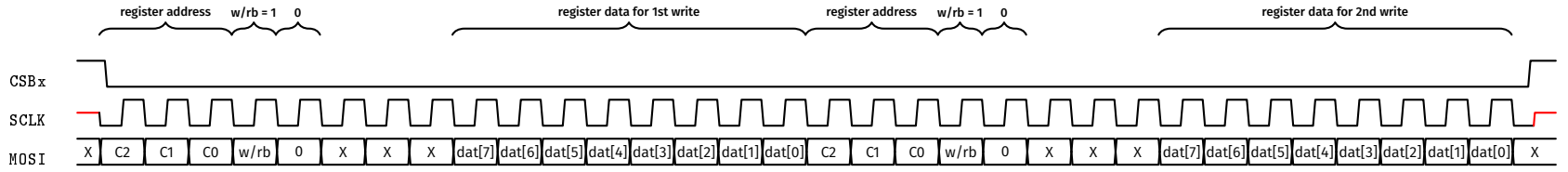


Figure 7: SPI timing specifications

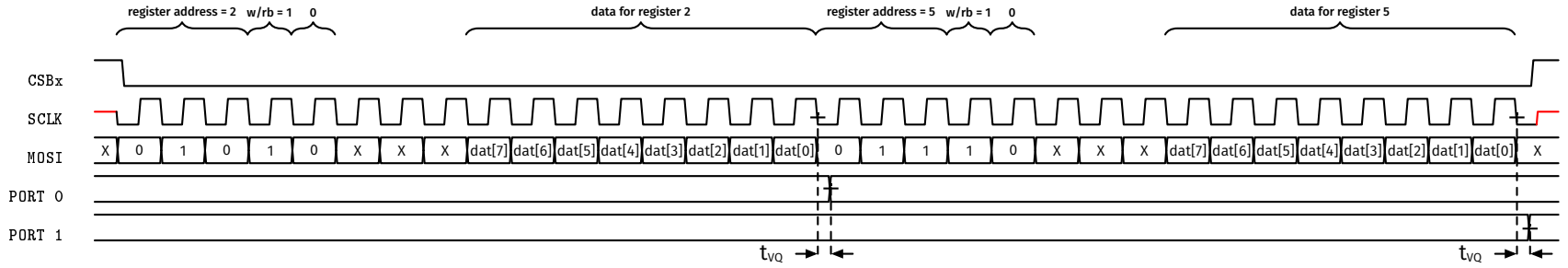


Figure 8: SPI example write register 2 then write register 3

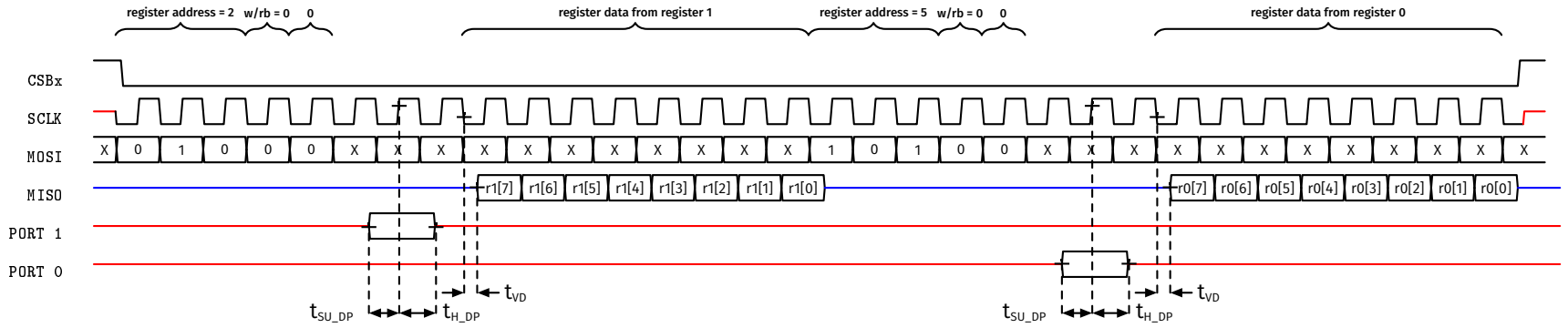


Figure 9: SPI example read register

Note: Red on SCLK, PORT 0 and PORT 1 indicates "don't care"
Blue on MISO represents "High Impedance"

6.9.2 SPI write

Refer to Figure 7 To write to the **APIO16** in SPI mode, CSBx must be brought low, at least $\mathbf{t_{SU\_CSB}}$ before the first rising edge of SCLK. Data is clocked into the MOSI pin on the rising edge of SCLK. Data must be present $\mathbf{t_{SU\_DAT\_SPI}}$ before each rising edge of SCLK and be held for a minimum of $\mathbf{t_{H\_DAT\_SPI}}$ after the rising edge of SCLK. The first data bit clocked in is C[2], then C[1] then C[0], which selects the register address to be written to. Next is the w/rb bit which indicates whether a register is to be read or written. The w/rb bit must be high to write to a register (NOTE: This is the opposite polarity from that used in I^2C mode) The next bit MUST be a zero and the following three bits are "don't care" bits. The following eight bits are the eight bit value to be written to the selected register. The new register value takes effect after a time $\mathbf{t_{VQ}}$ after the falling edge of the clock that occurs after the rising edge that clocked in the last data bit: dat[0]. CSBx must remain low until at least $\mathbf{t_{H\_CSB}}$ after that falling edge.

CSBx can remain low after the last falling edge and a new address and data value can be clocked in: it is not mandatory to cycle CSBx after each byte written, however, it is recommended that CSBx IS cycled after each data byte written. Please see the section on error conditions.

6.9.3 SPI read

Refer to Figure 9 In SPI mode, the A0/MISO pin is used as a MISO pin, providing data from the target to the controller. The MISO pin is tri-stated, except when it is required to send data back to the controller. To read from the **APIO16** in SPI mode, CSBx must be brought low, at least $\mathbf{t_{SU\_CSB}}$ before the first rising edge of SCLK. Data is clocked into the MOSI pin on the rising edge of SCLK. Data must be present $\mathbf{t_{SU\_DAT\_SPI}}$ before each rising edge of SCLK and be held for a minimum of $\mathbf{t_{H\_DAT\_SPI}}$ after the rising edge of SCLK. The first data bit clocked in is C[2], then C[1] then C[0], which selects the register address to be read from. Next is the w/rb bit which indicates whether a register is to be read or written. The w/rb bit must be low to read from a register. The next bit MUST be a zero and the following three bits are "don't care" bits. Next, the target changes the MISO pin from high impedance to actively drive data onto the MISO line at a time $\mathbf{t_{VD\_SPI}}$ after the next falling edge on SCLK. The desired eight bits of data to be read back is clocked out onto the MISO line, with data changing $\mathbf{t_{VD\_SPI}}$ time after the falling edge of the SCLK line. The data on MOSI is ignored during this time. The MISO line returns to high impedance $\mathbf{t_{VD\_SPI}}$ after the falling edge at the end of the last data bit on MISO, or $\mathbf{t_{DIS\_MOSI}}$ after CSBx goes high. CSBx can remain low after the last falling edge and a new address and data value can be clocked in: it is not mandatory to cycle CSBx after each byte written, however, it is recommended that CSBx IS cycled after each data byte written. Please see the section on error conditions.

Note: the polarity of the w/rb used in SPI is the opposite to the polarity used in I^2C

6.9.4 SPI read 4-wire

Multiple **APIO16** devices can be connected to the same MISO line. As long as only ONE **APIO16** device is requested to send back data at a time, there will be no bus conflicts on the MISO line. It is recommended to connect a pull up or pull down resistor onto the MISO line, to ensure that it does not float when no devices are addressed.

6.9.5 SPI read 3-wire

It is also possible to short the MISO and MOSI pins together and connect multiple devices to the same wire, provided both of the following conditions are met:

- Only ONE **APIO16** device is requested to send back data at a time.
- The controller tri-states its output driving the joined MISO/MOSI line at the appropriate time to ensure the controller and Target are not both driving the same line at the same time.

6.9.6 SPI read from port

In SPI mode, when reading from the port pins, the state of the port pins is latched on the 3rd rising SCLK edge after the w/rb bit is latched. To guarantee correctly latching the expected data on the pins, the data must be stable $\mathbf{t_{SU\_DP\_SPI}}$ before and remain stable $\mathbf{t_{H\_DP\_SPI}}$ after that clock edge.

6.10 REGISTER DESCRIPTIONS

In I^2C and in SPI mode, the internal register functionality is identical.

There are eight register addresses, as shown in Table 11. All eight registers can be read from, six of the registers can be read or written. Registers 0 and 1 can only be read.

Table 11: APIO16 registers

BIT NAME(S)			REGISTER	REGISTER	PROTOCOL	RESET
C2	C1	C0	NUMBER			DEFAULT
0	0	0	0	Input port 0	read	xxxx xxxx
0	0	1	1	Input port 1	read	xxxx xxxx
0	1	0	2	Output port 0	read/write	1111 1111
0	1	1	3	Output port 1	read/write	1111 1111
1	0	0	4	Polarity port 0	read/write	0000 0000
1	0	1	5	Polarity port 1	read/write	0000 0000
1	1	0	6	Configuration port 0	read/write	1111 1111
1	1	1	7	Configuration port 1	read/write	1111 1111

Reading register 0 returns the state of the pins on port 0. The MSB gives the state of P0_7, the LSB gives the state of P0_0. Reading register 1 returns the state of the pins on port 1. The MSB gives the state of P1_7, the LSB gives the state of P1_0. Writing to register 0 or register 1 has no effect.

Table 12: Input port 0 register (c[2:0] = 0)

Bit	7	6	5	4	3	2	1	0
Port Pin	P0_7	P0_6	P0_5	P0_4	P0_3	P0_2	P0_1	P0_0

Table 13: Input port 1 register (c[2:0] = 1)

Bit	7	6	5	4	3	2	1	0
Port Pin	P1_7	P1_6	P1_5	P1_4	P1_3	P1_2	P1_1	P1_0

Register 2 controls the output data for port 0. A "1" in the port makes the port pull high if the output on that pin is enabled, a "0" makes the port pull low if the output on that pin is enabled. Asserting POR VCCI or pulling RESETB low clears the register to the default state of all "1"s, i.e. all pins will pull high if enabled. The MSB of the register affects port pin P0_7, the LSB affects port pin P0_0. Reading register 2 gives the current setting for register 2.

Register 3 controls the output data for port 1. A "1" in the port makes the port pull high if the output on that pin is enabled, a "0" makes the port pull low if the output on that pin is enabled. Asserting POR VCCI or pulling RESETB low clears the register to the default state of all "1"s, i.e. all pins will pull high if enabled. The MSB of the register affects port pin P1_7, the LSB affects port pin P1_0. Reading register 3 gives the current setting for register 3.

Table 14: Output port 0 register (c[2:0] = 2)

Bit	7	6	5	4	3	2	1	0
Port Pin	P0_7	P0_6	P0_5	P0_4	P0_3	P0_2	P0_1	P0_0
Default	1	1	1	1	1	1	1	1

Table 15: Output port 1 register (c[2:0] = 3)

Bit	7	6	5	4	3	2	1	0
Port Pin	P1_7	P1_6	P1_5	P1_4	P1_3	P1_2	P1_1	P0_0
Default	1	1	1	1	1	1	1	1

Register 4 controls the polarity inversion for read of port 0. A "1" inverts the polarity of the bit which will be read back when register 0 is read. The MSB of the register affects the read for port pin P0_7, the LSB affects the read for port pin P0_0. Note that changing this bit does NOT affect the INTB state, it simply inverts or does not invert the polarity of bits read back when register 0 is read. Reading register 4 gives the current setting for register 4.

Table 16: Polarity port 0 register (c[2:0] = 4)

Bit	7	6	5	4	3	2	1	0
Port Pin	P0_7	P0_6	P0_5	P0_4	P0_3	P0_2	P0_1	P0_0
Default	0	0	0	0	0	0	0	0

Register 5 controls the polarity inversion for read of port 1. A "1" inverts the polarity of the bit which will be read back when register 1 is read. The MSB of the register affects the read for port pin P1_7, the LSB affects the read of port pin P1_0. Note that changing this bit does NOT affect the INTB state, it simply inverts or does not invert the polarity of bits read back when register 1 is read. Reading register 5 gives the current setting for register 5.

Table 17: Polarity port 1 register (c[2:0] = 5)

Bit	7	6	5	4	3	2	1	0
Port Pin	P1_7	P1_6	P1_5	P1_4	P1_3	P1_2	P1_1	P1_0
Default	0	0	0	0	0	0	0	0

Register 6 controls the output enables for port 0. A "1" in the port makes the port pin high impedance, a "0" enables the output on that pin. Asserting POR VCCI or pulling RESETB low clears the register to the default state of all "1"s, i.e. all pins are inputs. The MSB of the register affects port pin P0_7, the LSB affects port pin P0_0. Reading register 6 gives the current setting for register 6.

Table 18: Configuration port 0 register (c[2:0] = 6)

Bit	7	6	5	4	3	2	1	0
Port Pin	P0_7	P0_6	P0_5	P0_4	P0_3	P0_2	P0_1	P0_0
Default	1	1	1	1	1	1	1	1

Register 7 controls the output enables for port 1. A "1" in the port makes the port pin high impedance, a "0" enables the output on that pin. Asserting POR VCCI or pulling RESETB low clears the register to the default state of all "1"s, i.e. all pins are inputs.The MSB of the register affects port pin P1_7, the LSB affects port pin P1_0. Reading register 7 gives the current setting for register 7.

Table 19: Configuration port 1 register (c[2:0] = 7)

Bit	7	6	5	4	3	2	1	0
Port Pin	P1_7	P1_6	P1_5	P1_4	P1_3	P1_2	P1_1	P1_0
Default	1	1	1	1	1	1	1	1

6.11 APPLICATION CIRCUIT

6.11.1 Basic I²C operation

Please see Figure 10. For basic I²C operation, all that is necessary is to tie the A0, A2, A2, A3 pins high or low to program the desired target device address.

Ensure that SDA and SCL are connected to the I²C bus and have appropriately sized pullup resistors somewhere on those lines. Decoupling capacitors of at least 10nF should be within 25mm of the IC.

It is recommended that INTB is pulled up or pulled down through a resistor, even if this signal is not used. It is also acceptable to tie INTB directly to the VSS of the device.

The port pins P0_1 through P0_7 and P1_0 through P1_7 are configurable to be inputs and/or outputs as desired. If used as inputs, it is recommended to ensure that those pins are always driven or have a pull-up or pull down resistor

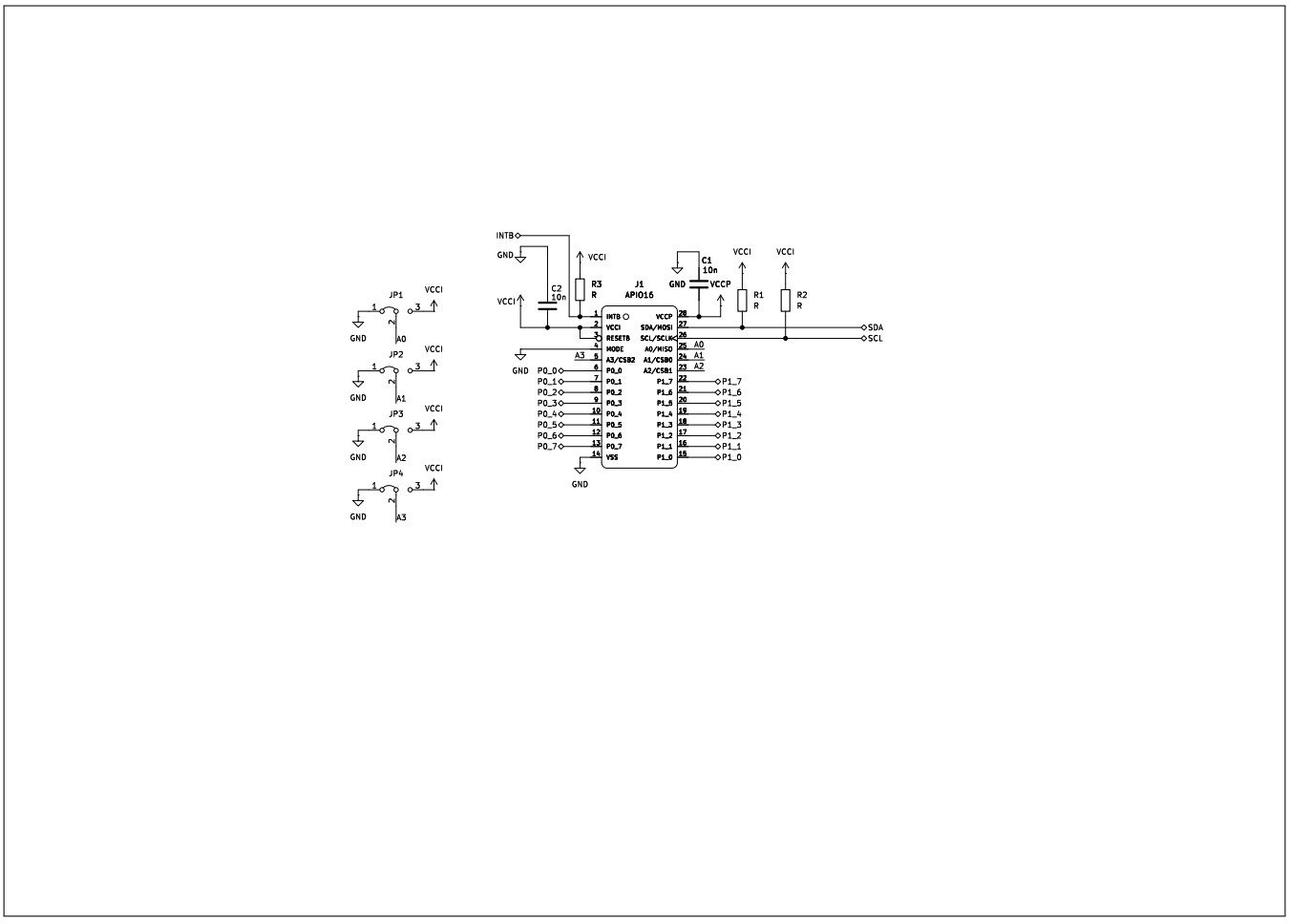


Figure 10: basic I²C application

6.11.2 I²C connection to FPGA low voltage bank

FPGA I/Os are grouped in banks, each bank can be tied to a different power supply. It is often the case that not all pins on a low voltage bank are used, there can be several pins un-used. Because the **APIO16** has level transation built in, it is possible to use these pins to control the **APIO16**. If the part is used in I²C mode, the SDA

and SCL pins would be pulled up to the VCCI rail, but note that INTB could be pulled up to a different, higher voltage if needed. The **APIO16** can reliably support operation on VCCI and/or VCCP down to 1.4V.

6.11.3 Sizing the pull-up resistors for SDA and SCLK for I²C

If the part is used in I²C mode, pull up resistors are required on the SCL and SDA lines. The resistors must be small enough to meet the required speed of operation and large enough that all the components connected to the I²C bus can pull the lines down to a sufficiently low voltage.

The bus capacitance is the total capacitance of wire, connections and pins. This capacitance limits the maximum value of the pullup resistors due to the maximum allowable rise time for the chosen speed of operation of the bus. Note that **APIO16** does not require operation at its maximum speed, the controller can run the bus at any speed it likes, provided the required timings are met. Table 20 details the maximum allowable rise time for SDA and SCL to support certain standard bus speeds.

Table 20: Standard I²C bus speed requirements

SYMBOL	PARAMETER	STANDARD MODE	FAST MODE	FAST MODE PLUS	UNIT
$t_{r(max)}$	rise time of SDA and SCL (30% to 70% of VDDI)	1000	300	120	ns

Given that the $t_{r(max)}$ is specified for thresholds of 30% to 70%, the maximum pullup resistance required can be calculated from the following equation:

$$R_{p(max)} = \frac{t_{r(max)}}{0.8473 \times C_b}$$

The minimum pullup resistance is limited due to the limited sink current of the devices on the bus, it can be calculated using:

$$R_{p(min)} = \frac{V_{CC} - V_{OL(max)}}{I_{OL}}$$

Where V_{CC} represents the supply that the I²C pull-up resistors are connected to.

Once the maximum and minimum allowable value of R_P has been calculated, the designer is free to select a value between these two limits: towards the high end if low current consumption is required, towards the lower end if higher noise immunity is desired.

6.11.4 Basic SPI operation

Please see Figure 11. For basic SPI operation, all that is necessary is to connect the VCCI to the same rail used by the controller for the SPI bus. Only one CSBx pin is needed, so CSB1 and CSB2 are shown here as tied to VSS.

Decoupling capacitors of at least 10nF should be within 25mm of the IC.

It is recommended that INTB is pulled up or pulled down through a resistor, even if this signal is not used. It is also acceptable to tie INTB directly to the VSS of the device. It is allowable to pull up INTB with a resistor tied to a higher rail than VCCI, within the maximum allowable limits for the INTB pin.

If read-back via MISO is not required, the MISO pin can be left disconnected, although it is recommended to tie the pin to VSS or VCCI with a pull up or pull down resistor of, 1k to 10k so that it does not float.

The port pins P0_1 through P0_7 and P1_0 through P1_7 are configurable to be inputs and/or outputs as desired. If used as inputs, it is recommended to ensure that those pins are always driven or have a pull-up or pull down resistor.

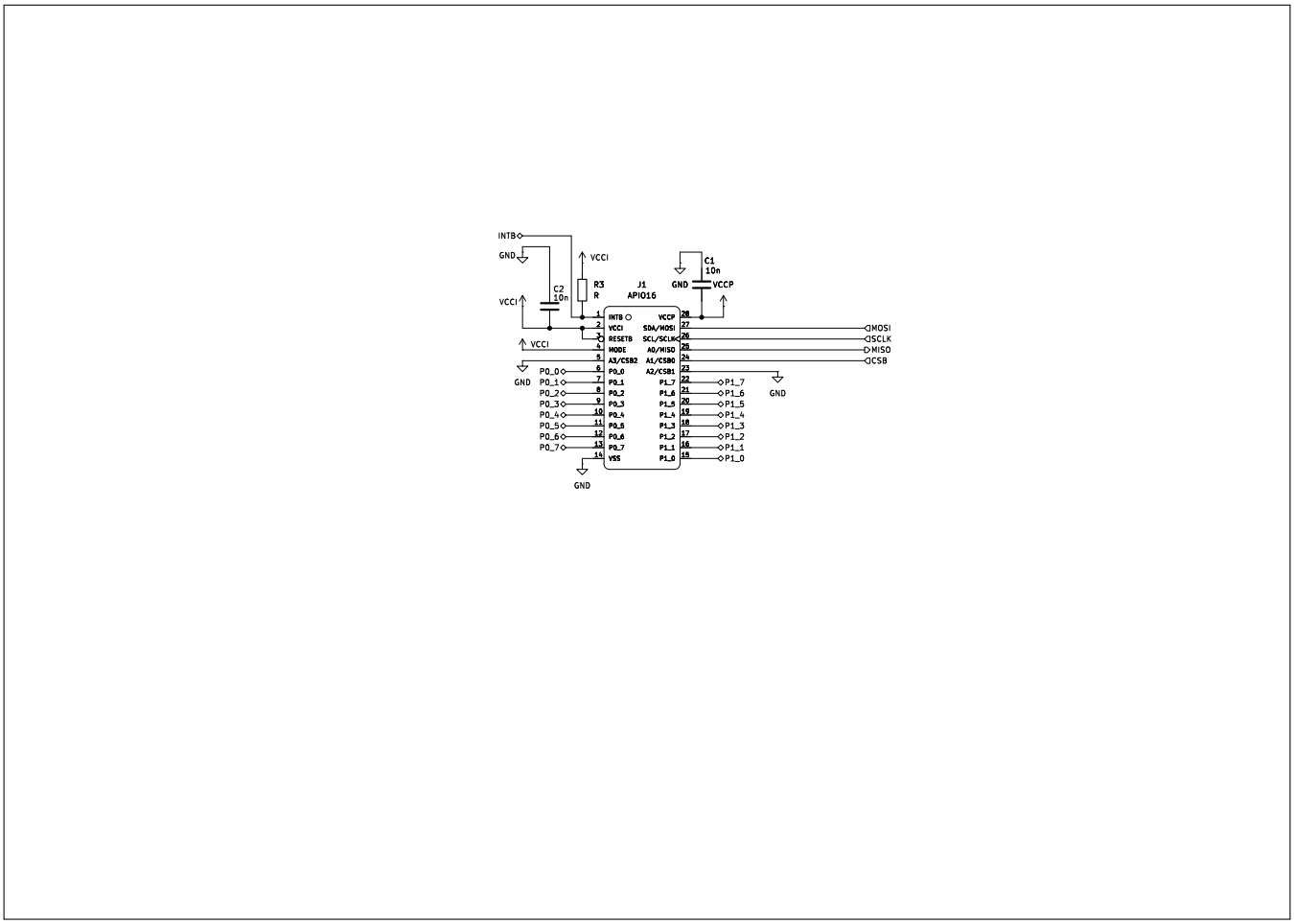


Figure 11: basic SPI application

6.11.5 Using CSB0, CSB1, CSB2 to multiplex many devices in SPI mode

In SPI mode, the CSBx = CSB0 OR CSB1 OR CSB2: all the CSBx pins bust be LOW to select the device. As a result, the extra CSBx pins can be used to enable selection of multiple **APIO16** devices with a minimum number of select lines.

6.12 LAYOUT GUIDELINES

A decoupling capacitor of 10nF to 100nF should be connected between VCCI and VSS. This capacitor should be located within 25mm of the IC. A similar capacitor should be placed between VCCP and VSS. If the port pins are going to source large currents, it may be necessary to add additional capacitance from VCCP to VSS.

6.13 ERROR HANDLING

In a high radiation environment, it is possible that the I^2C or SPI commands to the device are corrupted in some way. Here we define what the device will do in the event it can detect some sort of error.

6.13.1 I^2C illegal command

A valid command is an 8 bit word with the first five bits zero, the last three bits are the command itself. If any of the first five bits are NOT zeros, this will be detected as an illegal command. The device will ignore the command and wait until it detects a restart or a stop followed by a start or the device is reset by RESETB pulled low or a VCCI UVLO.

6.13.2 I^2C controller acknowledge fail

If the controller does not acknowledge a read byte, the device will stop sending data back on SDA and waits until it detects a restart or a stop followed by a start or the device is reset by RESETB pulled low or a VCCI UVLO.

6.13.3 I^2C target acknowledge fail

If the target ack fails to reach the controller because the bus is being held high by some bust fault condition, the target does not detect this. The target will wait for the controller to send the next address. The controller should detect the bus fault and issue a reset.

6.13.4 I^2C target data send to controller fail

The target does not monitor the data sent back to the controller. If some other device on the bus corrupts the data, the target will not detect this.

6.13.5 I^2C stop detect

If the target detects a stop at any time, it will stop whatever it is doing and wait for a start command.

6.13.6 I^2C start detect

If the target detects a start at any time, it will stop whatever it is doing and treat the start as a new start command.

6.13.7 SPI illegal command

A valid command is an 8 bit word. The first three bits are the command itself, followed by the w/rb bit then one zero and three "don't care" bits. If the zero after the w/rb bit is not present, this will be detected as an illegal command. The device will ignore the command and wait until it detects CSBx high then low or a RESETB pulled low or a VCCI UVLO.

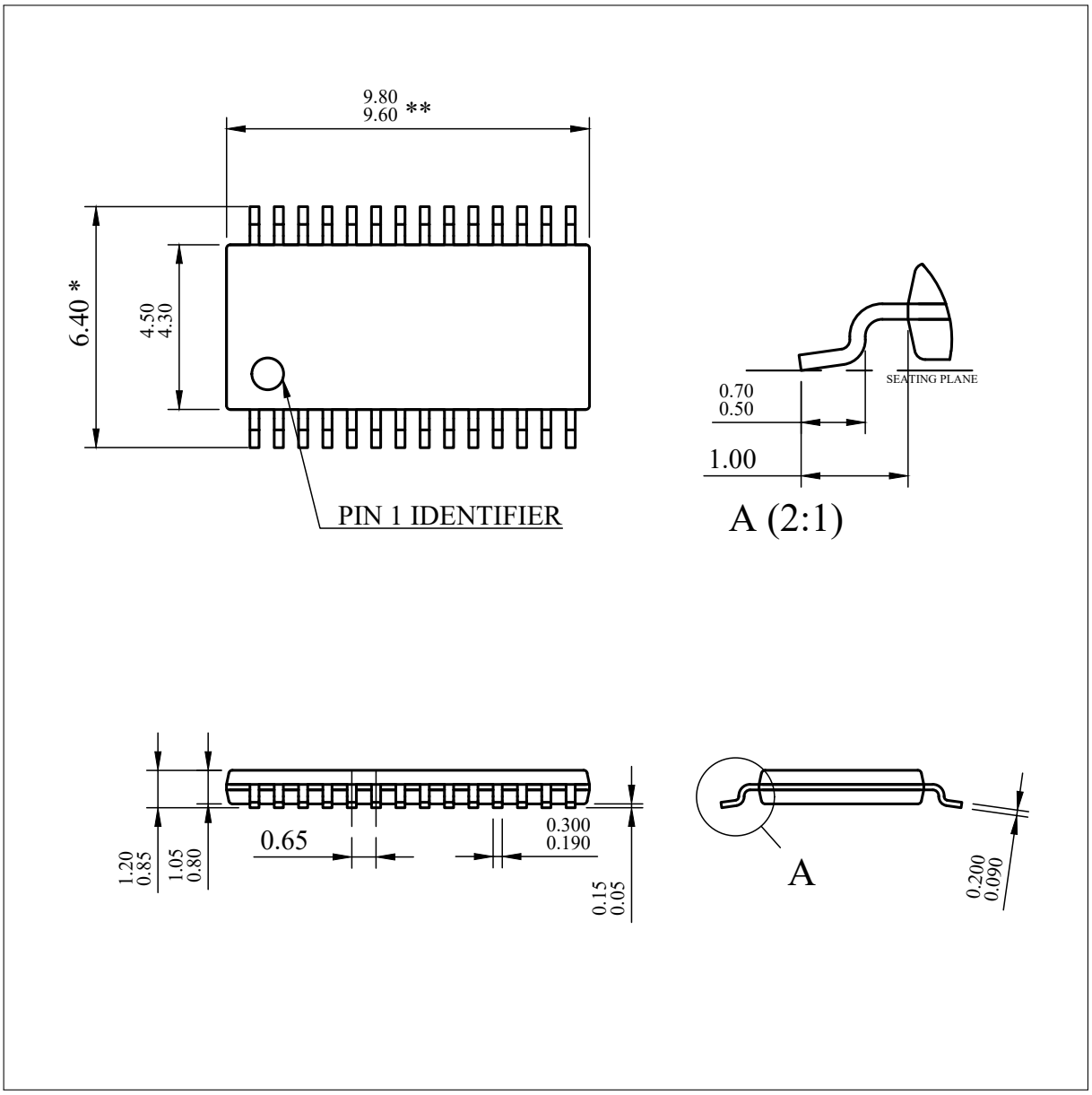
6.13.8 SPI loss of synchrony

SPI has the capability to accept data words continually WITHOUT pulling CSBx high then low. This can be used to stream data rapidly, however, there is a risk that a single event could corrupt the SCLK or SDAT and the device will lose its place in the data stream. Without CSBx pulling high then low, there is no way for the device to know when to resynchronize. It is therefore HIGHLY recommended that the user pull CSBx high then low to resynchronize all data words. If fast burst data is required, omit CSBx transitions for only as long as necessary, then resume CSBx transitions.

6.13.9 Extremely long transactions

All transactions should terminate with CSBx high (for SPI) or with a STOP in I^2C . If a transaction is paused without these terminating events, there is a very small risk of a combination of multiple single events over an extended period causing faulty operation. Note that this vulnerability would have a VERY small cross section due to the internal modular redundancy in the device. This small cross section failure mode is completely eliminated as long as each transaction terminates correctly in a timely manner.

7 PACKAGING INFORMATION



Notes:

1. All linear dimensions are in millimeters. Dimensioning and tolerancing are as per ISO/TS 128-71:2010
2. The part is compliant with JEDEC MO-153 specifications.

∗ Body width does **not** include interlead flash. Interlead flash shall not exceed 0.25mm each side.
∗∗ Body length does **not** include mold flash, protrusion, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0.15 mm on each side.

Figure 12: 28-NT - Package Mechanical Detail (NiPdAu)

8 ORDERING INFORMATION

Example part numbers for the APIO16 are listed in Table 21. The full list of options for this part can be found in Figure 13. Please contact Apogee Semiconductor sales at sales@apogeesemi.com for further information on sampling, lead time and purchasing on specific part numbers.

Table 21: APIO16 Ordering Information

DEVICE	DESCRIPTION	PACKAGE	LEAD FINISH	PACKAGE DIAGRAM	PACKAGE MASS
APIO16ANT-R	Radiation Hardened level translating I^2C, SMBUS, SPI I/O expander (30 krad (Si))	TSSOP-28	NiPdAu	28-NT	TBD
APIO16BNT-R	Radiation Hardened level translating I^2C, SMBUS, SPI I/O expander (30 krad (Si))	TSSOP-28	NiPdAu	28-NT	TBD
APIO16CNT-R	Radiation Hardened level translating I^2C, SMBUS, SPI I/O expander (30 krad (Si))	TSSOP-28	NiPdAu	28-NT	TBD
APIO16ENT-R	Radiation Hardened level translating I^2C, SMBUS, SPI I/O expander (for evaluation only)	TSSOP-28	NiPdAu	28-NT	TBD

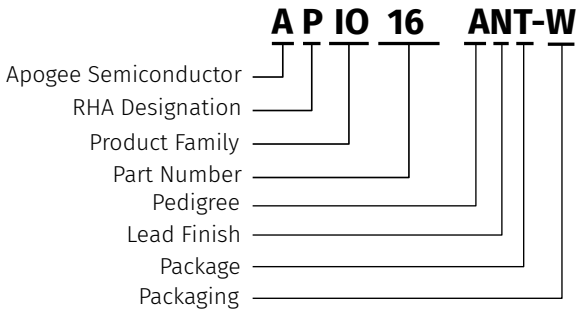


Figure 13: Part Number Decoder

1. RHA Designation
   - **P** 30 krad (Si)
   - **F** 300 krad (Si)
2. Product Family
   - **I/O expander**
3. Part Number
   - **16 number of bits**
4. Pedigree
   - **A** -55 to +125 °C (Burn-in)
   - **B** -55 to +125 °C (No burn-in)
   - **C** 25 °C (No burn-in)
   - **E** 25 °C Functional Test Only (Evaluation)
5. Lead Finish
   - **N** Nickel Palladium Gold (NiPdAu)
6. Package
   - **T** Thin Shrink Small Outline Package (TSSOP)
7. Packaging
   - **W** Waffle Pack or Pillow Stat Box
   - **R** Tape and Reel[1]
   - **J** JEDEC Tray

[1] Contact us for custom reel quantities. Orders less than full reel quantities may be shipped as cut tape.

9 REVISION HISTORY

REVISION	DESCRIPTION	DATE
A04	added TID and SEE from testing, adjusted drive strengths, changed GND to VSS, various parameter updates	2025-FEB-06
A03	removed NDA restrictions, added typical quiescent	2024-SEP-09
A02	Added 1.4V support, adjusted POR voltage down, additional characteristics, fixed simplified IO schematic	2024-AUG-23
A01	Full preliminary datasheet initial release.	2024-JUL-01
A00	Onesheet initial release.	2023-DEC-01

For the latest version of this document, please visit https://www.apogeesemi.com.

10 LEGAL

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