

## 1. Type of Change (Major or Minor)

Major

## 2. Change Description

### **AP54RHC504 and AP54RHC505 changes:**

- a) Quiescent supply current ( $I_{CCA}$ ) max limit change from  $18\mu\text{A}$  to  $30\mu\text{A}$ .
- b) Low-level output voltage change ( $V_{OL}$ ),  $I_O = 1\text{mA}$ ,  $V_{CCY} = 1.65$  to  $5.5\text{V}$ . Change max limit from  $0.1\text{V}$  to  $0.15\text{V}$ .
- c) Changes to POR descriptions with respect to  $V_{CCY}$ 
  - Description update to include  $V_{CCY}$  in POR behavior
  - Update logic truth table to include both  $V_{CCA}$  and  $V_{CCY}$  states
  - Detailed description to update to include recommendation to power  $V_{CCY}$  prior to  $V_{CCA}$  to prevent unwanted potential glitch during power up.

### **AP54RHC505 Changes:**

- d) Added verbiage indicating the the bus keeper functionality is active on all inputs and outputs.
  - Removed statement indicating that EN (now OE) does not have bus keeping on input.

## 3. Impact on Product and/or Process

- a) Limit increase for  $I_{CCY}$  will prevent marginal yield loss.
- b) Limit increase for  $V_{OL}$  will prevent marginal yield loss during high temperature testing.
- c) No product/process impact.
- d) No product/process impact.

## 4. Justification for Change

- a) Adjust limits to accurately reflect device current requirements and limits.
- b) Adjust limits to accurately reflect device  $V_{OL}$  drive capability at  $1\text{mA}$  loading.
- c) Accurately reflect device behavior with respect to POR and  $V_{CCY}$  biasing.
- d) Accurately reflect AP54RHC505 bus keep functionality and associated pins.

## 5. Change Risk Assessment

- a) No risk, increase in current is minimal.
- b) Minimal to no risk,  $V_{OL}$  at these conditions well within standard  $V_{IL}$  levels at  $V_{CC}$  nodes down to 1.65V.
- c) Potential risk to customer applications intending to keep  $V_{CCY}$  powered during cold spare operations. Potential risk to customer applications that are sensitive to potential power up glitch on outputs.
- d) Minimal potential risk to customer applications that utilize multiple AP54RCH505 tied together on output bus. The minimal additional bus keep current per output must be accounted for to insure driver is capable of driving the additional loading. Minimal potential risk of utilizing the OE pin with bus keep functionality from extremely weak driver.

## 6. Qualification Plan

No qualification required. No changes to device process.

## 7. Qualification Report

N/A

## 8. Summary

See Change Description

## 9. Impacted Device - Document - Process List

AP54RHC504ELT, AP54RHC504ALT, AP54RHC504BLT, AP54RHC504CLT, AP54RHC505ELT, AP54RHC505ALT, AP54RHC505BLT, AP54RHC505CLT

## 10. Sample Availability Date and Projected Production Shipment

a) b) **Sample availability date:** N/A. Please contact Apogee for samples if needed.

**Projected production shipment date:** December 24, 2024 or upon PCN approval.

c) d) Informational notification. No change to material or testing.

## 11. File Attachment

N/A.

Apogee Semiconductor

PCN-11

AP54RCH504 AP54RCH505 Datasheet update: ICCA, VOL 1ma, POR description.

Version: 1.0