Accelerate your Analog FinFet Rad Hard Design Using ADONIS™

Silicon Technologies is offering a four-hour training session at RHET to demonstrate the advantages of the ADONIS™ technology through the design of a 200MHz 8-bit DAC. We will show the student how to proceed from a paper schematic to move through all the microelectronics design phases which would normally take 6-12 people months to completing the circuit ready to be taped out as an IP block.

We will start by designing the DAC from scratch, simulate, lay out, perform DRC and LVS, extract, and complete an extracted simulation of the design. We will also show how Reliable Microsystems' VIRAD tool can predict radiation hardness and how it fits into the ADONIS™ framework.

The basic principles of the DAC being designed will be discussed, but the focus of the class will be on the advantages of the ADONIS™ technology. We will be using the Global Foundry 12nm process for the design.

The instructor for the class is Whitney Durham, who has over 20 years of experience in the design of robust ASICs. She is currently serving as Director of ASIC Development at Silicon Technologies Inc.

What You Will Learn

- How to use the ADONIS™ technology to design a 200MHz 8-bit DAC to develop a complex Analog Circuit from scratch to ready to be taped out IP block in an afternoon.
- How to predict radiation hardness using both the ADONIS™ and the VIRAD tool, and to learn when to use each
- How to simulate, lay out, and verify for DRC and LVS on a DAC design
- The basic principles of DAC design

The Live training will be held at the Marriott Allen Hotel, Allen, Texas, in conjunction with RHET 2023. It will begin at 1:00 and end at 5:00 with afternoon refreshments. All equipment will be provided.

Silicon Technologies can offer 20 training seats. Please RSVP to Whitney Durham, wdurham@silicontech.us by October 6.

Please reserve your RHET Marriott hotel and register for RHET at www.apogeesemi.com/RHET2023