

Military

EMBEDDED SYSTEMS

@military_cots

www.MilitaryEmbedded.com

John McHale
Mike Hopper's impact

5

Special Report
Hardening GPS

16

Mil Tech Trends
Converting ocean waves into power

36

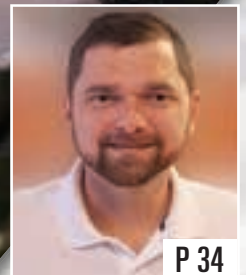
Industry Spotlight
CMOSS brings speed, cost benefits

40

Nov/Dec 2021 | Volume 17 | Number 8

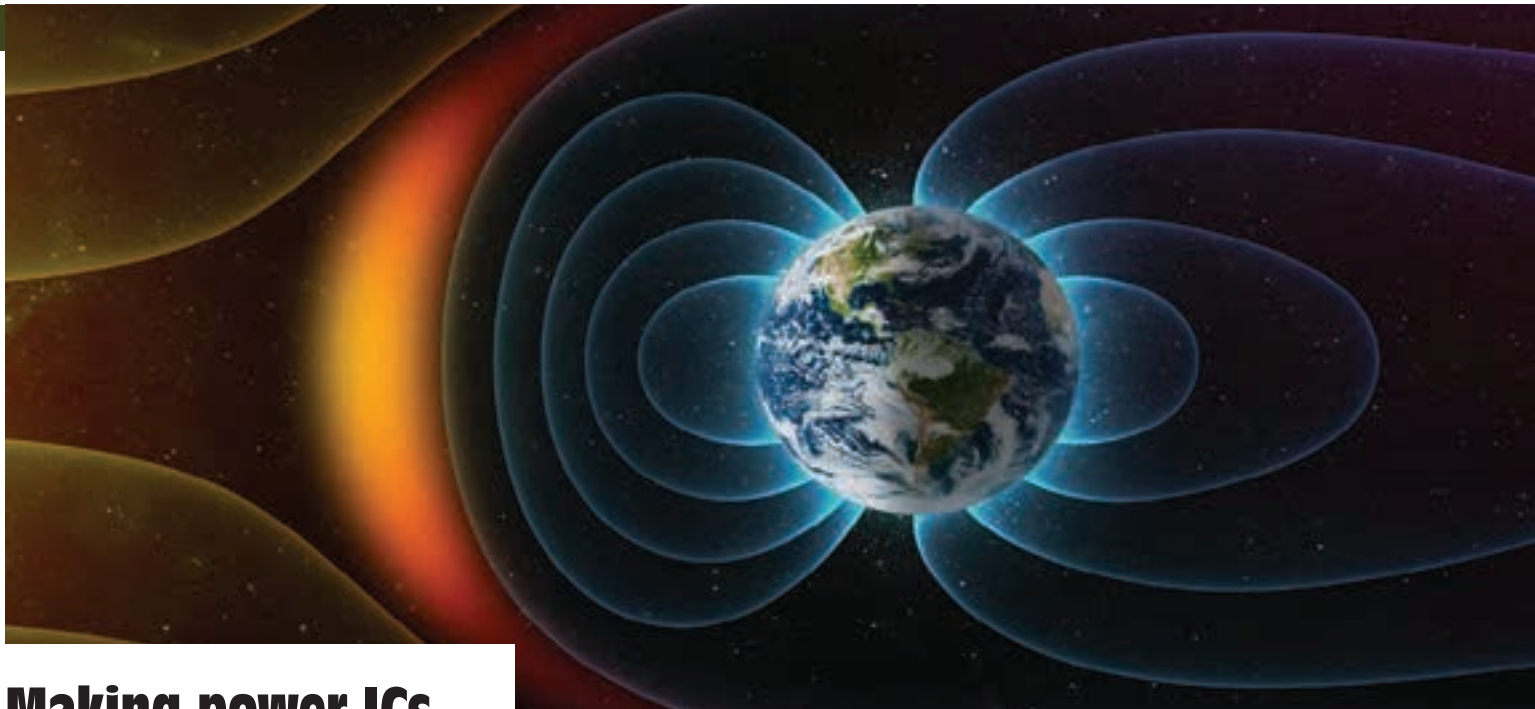
SOLDIERS IN GPS-DENIED ENVIRONMENTS REQUIRE SENSOR-POWERED NAVIGATION TECH

P 10



P 34

Making power ICs more affordable
By Anton Quiroz,
Apogee Semiconductor



Making power ICs more affordable

By Anton Quiroz

To enable the space systems of the future, and to make space more accessible, first the industry must solve the problems with rad-hard semiconductors. There are a number of major cost drivers for space-grade power integrated circuits (ICs) that need to be addressed.

Radiation-hardened integrated circuits (ICs) needed for space applications are large, expensive, and lag state-of-the-art performance by more than a decade. The factors driving these realities include the extensive testing required for space-grade parts, a dwindling supply of legacy devices, the high cost of designing rad-hard integrated circuits, and the high cost of hermetic ceramic packaging.

How to make power rad-hard ICs more affordable? I remember my first years working in business development for a high-reliability product line developing ICs for space applications. As I was familiarizing myself with the product portfolio and customers, I noticed significant sales coming from what I considered to be “legacy” products. Many of these parts – designed back in the 1980s and

1990s – were still being designed into new systems. Moreover, power ICs that normally went for about \$2 in volume for commercial applications would sell for over \$2,000 in the rad-hard space.

High cost of testing

Most radiation-hardened integrated circuits are tested and qualified per MIL-STD-883 and MIL-PRF-38535. These are common standards that have been utilized by the high-reliability industry for more than 20 years.

While these standards helped the government and suppliers avoid managing sometimes hundreds of custom specs for the same product, the pricing still did remain high compared to the equivalent commercial functions due to the extensive testing and screening required on the space-grade products.

Testing costs very often swamped the material costs. Some IC testing can run hundreds of dollars on ICs that cost less than one dollar to manufacture. This testing versus manufacturing cost disparity is even more pronounced with plastic devices. This extra testing is supposed to increase the reliability of the components.

The high-reliability industry has been evaluating more reliable commercial flows such as automotive (AEC-Q100) and enhanced plastic (V62), which leverage the process monitors that make these commercial products more reliable without the expensive 100% screening normally required for space-grade product.

Due to the lack of state-of-art electronics for space applications, many customers resort to upscreening commercial devices. Upscreening – which involves testing commercial off-the-shelf (COTS) parts to see if they conform to military specifications – often costs hundreds of thousands of dollars and must be done for every new lot of devices. There is also no guarantee that the parts will work; moreover, the upscreening process itself can lead to reliability issues such as latent defects. With power devices, finding commercial ICs that are “rad-hard by serendipity” and suitable for upscreening is even more difficult. This situation arises because power ICs are subjected to higher voltages and are susceptible to catastrophic single-event-effects caused by heavy ions in space and to the

degradation caused by total ionizing dose (TID) effects.

Efforts are underway to standardize a space plastic flow as part of MIL-PRF-38535 specification. The "Class P" standard is under consideration by government agencies and industrial partners. While this standard is a step in the right direction, it does plan to incorporate some expensive screening steps such as 100% burn-in, 100% x-ray, and serialized data logs: all of these manually done, expensive processes.

Dwindling supply

Many of the older space-grade components are on die bank, which means they can no longer be manufactured and supply is therefore limited. Supply limitations normally happen when a wafer-fabrication facility shuts down a process due to lack of business viability or for upgrade purposes. Sometimes the processes get transferred to a new fabrication facility, but more often than not the process is obsoleted all together. Even in cases where processes get transferred to new facilities, that move can lead to an IC that is electrically equivalent but with vastly different radiation performance.

Dwindling supply of these older components means that production programs are at risk and the price of components will continue to increase.

High cost of hermetic ceramic packaging

Traditionally, space-grade components are packaged in hermetic ceramic packages. Hermetic packages protect the die against moisture but are often 100 times more expensive than plastic packages and also negatively affect the components' performance. Customers, including government customers, are spending tens of millions of dollars developing digital application-specific ICs (ASICs) in smaller, higher-performing process nodes but are using suboptimal packages. These ceramic packages introduce large amounts of resistance and inductance with their longer leads and/or large redistribution layers. For rad-hard power ICs, the performance degradation introduced by these packages is even more apparent.

For state-of-the art components, commercial manufacturers ditched traditional packages years ago, opting for wafer chip scale packaging (WCSP). Wafer chip scale enables near-ideal die-to-board connection through a redistribution of layers and wafer bumps. WCSP reduces parasitic resistance and inductance that negatively affect the efficiency and performance of power ICs. Unfortunately, because of the disparity between the thermal coefficient of the die compared to the boards used for flight, WCSP is currently not accepted for spaceflight applications. The high amounts of thermal cycles necessary to qualify a space-grade device leads to solder-joint reliability with WCSP.

In order to drive the cost down and performance up, newer packaging techniques must be explored for space applications. There are efforts ongoing with various suppliers to improve packaging, but they are not yet qualified. Moving forward, some new suppliers have decided to only release space-grade parts in plastic – a good trend to see more widely adopted among satellite and spacecraft developers, especially those in the New Space market.

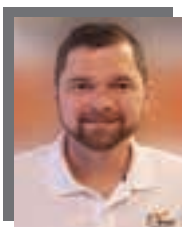
High cost of rad-hard IC design

It costs millions of dollars to design and productize even a so-called simple IC. If it needs to be rad-hard, it will be at least three times more expensive. IC design requires highly specialized, very expensive, computer-aided design (CAD) tools, which use components and models developed by the fabrication site and are specific to the process node. ICs sometimes have millions of transistors spread through hundreds of schematics and subsystems. The CAD tools, as well as proper verification, are the main reason complicated ICs have even a remote chance of first-pass success.

The issue is that rad-hard design breaks these tools. The unique layouts and modification required for rad-hard performance causes these tools to spit out thousands of design-rule violations. Inside these thousands of design-rule violations can lurk something critical, like a short-circuit or a bad connection. In addition to design-rule checkers not working properly, the layout-versus-schematic checks that ensure the components are hooked up correctly also do not function due to rad-hard modification. Without proper working tools, chances of success are 0². This means that rad-hard IC designers first have to invest many years and millions of dollars to work with the fabrications facilities to modify these tools to work properly for rad-hard design.

Using the proprietary TalRad [Transistor-Adjusted-Layout for Radiation] process, Apogee Semiconductor is developing a rad-hard hybrid analog/digital PWM [pulse-width modulation] controller to drive GaN [gallium nitride] and silicon FETs [field-effect transistors] that rival commercial state-of-art performance. This work is partially funded by NASA and is being developed in collaboration with NASA Jet Propulsion Laboratories.

Even while lowering the design and packaging cost, test costs still dominate the recurring cost of integrated circuits. This is where the industry has to think about using the process monitors utilized by automotive process flows and trim the screening flows to optimize the cost and reliability. The good news is that suppliers are pushing to reduce the cost of rad-hard components, making them more accessible for New Space customers. **MES**



Anton Quiroz, CEO of Apogee Semiconductor, has more than 16 years of experience in the semiconductor industry and over a decade in the aerospace and defense industry. Anton has held various management positions at Cobham Advanced Electronics Solutions and at Texas Instruments. He graduated summa cum laude from the University of Florida with a bachelor's degree in electrical engineering.

Apogee Semiconductor • <https://apogeesemi.com/>

Lead-times less than 2-weeks for most parts and quantities



The **AP54RHC** series is a family of radiation-hard logic and special functions designed to address the unique challenges faced by satellite systems architects. It is fabricated on a 180nm CMOS process utilizing proprietary hardening techniques, delivering high SEE resiliency and TID performance up to 30 kRad (Si) for LEO applications. The **AF54RHC** family has the same functionality as the **AP54RHC** products with improved TID resilience of 300 kRad (Si). All members of the **AP54RHC** and **AF54RHC** family operate across a full 1.65V to 5.5V range providing the system designer flexibility in logic-level interfaces. Additionally, zero-power penalty cold-sparing is offered on every input and output along with Class 2 ESD protection.

Part Number	Package	Pins	Description	Lead Finish	TID	SEL
AP54RHC301	TSSOP	14	Dual 3-input majority voter with error output	SnPb	30 kRad (Si)	80 MeV/mg/cm ²
AP54RHC504	TSSOP	14	5 channel level translator	SnPb	30 kRad (Si)	80 MeV/mg/cm ²
AF54RHC504*	TSSOP	14	5 channel level translator	SnPb	300 kRad (Si)	80 MeV/mg/cm ²
AP54RHC505	TSSOP	14	5 ch buffer level translator with bus hold	SnPb	30 kRad (Si)	80 MeV/mg/cm ²
AP54RHC705*	TSSOP	14	Dual D-Flip Flop with asynchronous clear	SnPb	30 kRad (Si)	80 MeV/mg/cm ²
AP54RHC506	TSSOP	14	5 channel 100 MHz transceiver	SnPb	30 kRad (Si)	80 MeV/mg/cm ²

7400 Series Logic Functions

AP54RHC00	TSSOP	14	Quad 2-input NAND	SnPb	30 kRad (Si)	80 MeV/mg/cm ²
AP54RHC02	TSSOP	14	Quad 2-input NOR	SnPb	30 kRad (Si)	80 MeV/mg/cm ²
AP54RHC32	TSSOP	14	Quad 2-input OR	SnPb	30 kRad (Si)	80 MeV/mg/cm ²
AP54RHC86	TSSOP	14	Quad 2-input XOR	SnPb	30 kRad (Si)	80 MeV/mg/cm ²
AP54RHC132*	TSSOP	14	Quad Schmitt 2-input NAND	SnPb	30 kRad (Si)	80 MeV/mg/cm ²
AP54RHC27	TSSOP	14	Triple 3-input NOR	SnPb	30 kRad (Si)	80 MeV/mg/cm ²
AP54RHC10	TSSOP	14	Triple 3-input NAND	SnPb	30 kRad (Si)	80 MeV/mg/cm ²
AP54RHC04	TSSOP	14	Hex inverter	SnPb	30 kRad (Si)	80 MeV/mg/cm ²
AP54RHC14*	TSSOP	14	Hex Schmitt inverter	SnPb	30 kRad (Si)	80 MeV/mg/cm ²
AP54RHC08	TSSOP	14	Quad 2-input AND	SnPb	30 kRad (Si)	80 MeV/mg/cm ²
AP54RHC11	TSSOP	14	Triple 3-input AND	SnPb	30 kRad (Si)	80 MeV/mg/cm ²
AF54RHC11*	TSSOP	14	Triple 3-input AND	SnPb	300 kRad (Si)	80 MeV/mg/cm ²
AP54RHC05	TSSOP	14	Hex open-drain inverter	SnPb	30 kRad (Si)	80 MeV/mg/cm ²

*Samples Only

Semiconductor Solutions for Harsh Environments™

www.apogeesemi.com

538 Haggard St. Ste 406

Plano, TX 75074

Contact us: sales@apogeesemi.com