Product Qualification Report

AP54RHC Family

This report covers the qualification results for the devices in the AP54RHC product family. The AP54RHC RadHard logic family is based on Apogee Semiconductor's Transistor-Adjusted-Layout for Radiation (TalRad™) design methodology that improves the radiation performance of commercial process technologies, enabling the rapid creation of rad-hard designs in a fraction of the time and effort.

The AP54RHC family includes functions such as level-translators, majority voters, transceivers and other 7400 series logic functions. The family is designed for class 2 ESD and specified for operation over a -55°C to +125°C temperature range and a 1.65V to 5.5V VDD range.

A single top-level metal layer is used to set the Boolean functionality and is the only difference between die in the members family.

1 Overview

Product	AP54RHC
Silicon Site	TSI Semiconductors
Assembly Site	Microchip MMT Thailand
Pin Count	14
Package Type/ Designation	TSSOP
Wirebond Material	Au 1.0 mils
Bond Type	Au Ball Bond
Mold Compound	G600V
Underfill/ Die Attach	2200D
MSL	1
Use Case Conditions	-55C to 125C
Test Revision	1.0.3
Die Size (X, Y)	(1353um, 2097um)
Die Thickness	15 mils
Lead Finish	Electroplated SnPb

2 Qualification Data Summary

Test	Conditions	Duration	Sample Size	Pass	Fail
HAST	JESD22-A110 130C/85%RH/33.3psia, Cond. A	96 hrs	48	48	0
HTOL	MIL-STD-883, TM 1005, Condition D	1000 hrs	48	48	0
TID	<= 45krad	n/a	14	14	0
SEL	Xe, LET 80 (MeV*cm^2)/mg,Fluence 1e7 Ions/cm^2	n/a	2	2	0
ESD (HBM)	<= 4000V	n/a	12	12	0
ESD (CDM)	<= 750V	n/a	12	12	0
Latch-up	JESD78, 10ms, 1.5*Vmax(operating)	n/a	40	40	0
MSL	Bake 24h at 125C, 168h Moisture Soak 85C/85% RH, 3x IR Reflow Sim 260C	n/a	30	30	0
Temperature Cycling	MIL-STD-883, Method 1010, Condition B, -55°C to 125°C	500 Cycles	48	48	0

Detailed reports available upon request

3 Packaging Level Qualification Data

Operation	Description	Sample Size	Spec. Limit	Pass/Fail
Die Attach	BLT	10 Units (4 Side/Unit)	0.30 - 1.50 mils	Pass
Die Attach	Die Shear Strength	35 Reading/Lot	MIN 3.0 KGF	Pass
Wire Bond	Wire Pull Strength	5 Units, All Wires	MIN 3.0 GMS	Pass
Wire Bond	Ball Shear Strength	5 Units, All Wires	MIN 35 GMS	Pass
Wire Bond	Loop Height	8 Units (4 Wire/Unit)	4.0 - 8.0 mils	Pass
Wire Bond	Cratering Test	3 Units All Pad	ACC/REJ : 0/1	Pass
Mold	Wire Sweep	30 Units (1 Reading/Unit)	Max 15%	Pass
Plate	Plating Thickness	35 Reading/Lot	0.3 - 0.8 mils	Pass
Plate	Plating Composition	35 Reading/Lot	80% - 90% (Sn)	Pass

Detailed reports available upon request

4 Preliminary FIT Rate Calculation

Preliminary FIT Rate was calculated using 48 samples with 1000hrs of HTOL testing and zero failures. This rate is expected to be lowered with extended HTOL testing to 4000hrs and qualification of future lots.

Confidence Level = 95%/60%
Sample Size = 48 Units
HTOL Duration = 1000 Hours
Device Hours = 48000
Failures = 0
E_a = 0.7 eV
FIT Rate = 67.47/20.64

5 Foundry Reliability Data - 0.18 um HVCMOS Analog Mode

Evaluation	Tested Device	Test Level	Duration per stress condition	Result (Pass/ Fail)	Failure Analysis
LV NFET Analog Mode Hot Carrier	1.8V NFET	Wafer	≈ 10hours	Pass	Not necessary
	1.8V NFETI	Wafer	≈ 10hours	Pass	Not necessary
	5V NFETM	Wafer	≈ 10hours	Pass	Not necessary
	5V NFETIM	Wafer	≈ 10hours	Pass	Not necessary
	1.8V NFET High Vt	Wafer	≈ 10hours	Pass	Not necessary
	1.8V NFETI High Vt	Wafer	≈ 10hours	Pass	Not necessary
LV PFET Analog Mode Hot Carrier	1.8V PFET	Wafer	≈ 10hours	Pass	Not necessary
	1.8V PFETI	Wafer	≈ 10hours	Pass	Not necessary
	5V PFETM	Wafer	≈ 10hours	Pass	Not necessary
	5V PFETIM	Wafer	≈ 10hours	Pass	Not necessary
	1.8V PFET High Vt	Wafer	≈ 10hours	Pass	Not necessary
	1.8V PFETI High Vt	Wafer	≈ 10hours	Pass	Not necessary

This table provides information about the Transistor Analog Mode's reliability test results of the TSI Semiconductor 0.18um HVCMOS technology at the Roseville fabrication facility. Since the estimated lifetime (MTTF) for Id_{analog} & GmMAX are at ≈ 89 years & ≈ 23.5 years respectively at 100% duty cycle, the transistors being utilized meet the targeted > 10 years lifetime criteria in analog mode with 100% duty cycle for this device. Note: If the component is not repairable then **MTTF=MTBF**

6 Conclusion

Based on HTOL data and foundry process qualification data, the FIT Rate is expected to reduce significantly as HTOL testing is extended from 1000 hours to 4000 hours. Once extended, these 48 samples will undergo 192000 device hours resulting in an estimated FIT rate of 16.87. Also, an additional 48 devices are being subjected to HTOL testing, which will further reduce the FIT rate. This report will be updated once additional HTOL testing is completed.

7 Revision History

REVISION	DESCRIPTION	DATE
A00	Initial internal release.	May 4, 2021

8 Legal

All product, product specifications and data are subject to change without notice. Apogee Semiconductor provides technical data (such as datasheets), design resources (including reference designs), reliability data (including performance in radiation environments), application or other design advice, safety information, and other resources **"as is"** and with all faults, and disclaims all warranties, express and implied, including without limitation any implied warranties of merchantability, fitness for a particular purpose or non-infringement of third party intellectual property rights. These resources are intended for skilled engineers with understanding of high reliability and high radiation environments and its complexities. Apogee Semiconductor is not responsible for: (1) selecting the suitable products for a given application, (2) designing, verifying, validating and testing it, or (3) ensuring that it meets any performance, safety, security, or other requirements. These resources are subject to change without advance notice. The use of these resources is restricted to the development of an application that uses the Apogee Semiconductor products described in them. Other reproduction and display of these resources is prohibited. No license is granted to any other Apogee Semiconductor intellectual property right or to any third-party intellectual property right. Apogee Semiconductor disclaims responsibility and reserves the right to demand indemnification for any claims, damages, costs, losses, and liabilities arising out of wrongful use of these resources. The products are provided subject to Apogee Semiconductor's Terms of Sale (https://www.apogeesemi.com/terms) or other applicable terms provided in conjunction with applicable products. The provision of these resources does not expand or otherwise alter applicable warranties or warranty disclaimers for Apogee Semiconductor products. Purchasers of these products acknowledge that they may be subject to and agree to abide by the United States laws and regulations controlling the export of technical data, computer software, electronic hardware and other commodities. The transfer of such items may require a license from the cognizant agency of the U.S. Government.