Radiation-Hardened Dual 3-Input Majority Voter

with **cold sparing**

1 GENERAL DESCRIPTION

The **AP54RHC301** is a radiation-hardened by design **dual 3-Input majority voter** that is ideally suited for commerical space and other applications demanding radiation tolerance and high reliability. It is fabricated in a 180 nm CMOS process utilizing proprietary radiation-hardening techniques, delivering high resiliency to single-event effects (SEE) and to a total ionizing dose (TID) up to **30 krad (Si) at 5 V** and **70 krad (Si) at 3.3 V**.

This device is a member of the Apogee Semiconductor AP54RHC logic family operating across a voltage supply range of **1.65 V to 5.5 V**.

The AP54RHC301 is an unique discrete majority voter logic function that offers two instances of a triple-input voter gate, with individual error outputs. In addition, a dedicated “error detected” indication is available, in addition to an external error input signal.

Zero-power penalty™ cold sparing is supported, along with Class 2 ESD protection on all inputs and outputs. A proprietary output stage and robust power-on reset (POR) circuit allow the AP54RHC301 to be cold-spared in any redundant configuration with no static power loss on any pad of the device. The redundant output stage also features a high drive capability with low static power loss.

The AP54RHC301 also features a triple-redundant design throughout its entire circuitry, which allows it to be immune to single-event transients (SET) without requiring additional redundant devices.

Ordering information may be found in Table 9 on Page 13.

1.1 FEATURES

- **1.65 VDC to 5.5 VDC** operation
- Inputs tolerant up to 5.5 VDC at any V_{CC}
- Provides logic-level down translation to V_{CC}
- Extended operating temperature range (-55 °C to +125 °C)
- Proprietary **cold sparing capability** with **zero** static power penalty
- **Built-in triple redundancy** for enhanced reliability
- Internal power-on reset (POR) circuitry ensures reliable power up and power down responses during hot plug and cold sparing operations
- Class 2 ESD protection (4000 V HBM, 500 V CDM)
- TID resilience of **30 krad (Si)** assured at 5.5 V and characterized to **70 krad (Si)** at 3.3 V.
- SEL immune to LET of **80 MeV-cm^2/mg**
- Meets NASA’s ASTM E595 outgassing specification

1.2 LOGIC DIAGRAM

The AP54RHC301 logic function is shown below:

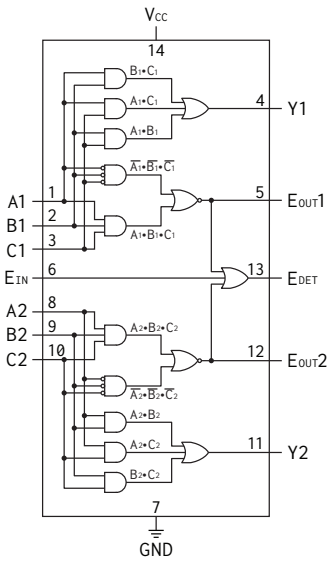

Figure 1: AP54RHC301 Logic Diagram

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2 ACRONYMS AND ABBREVIATIONS

ESD	Electrostatic Discharge
POR	Power On Reset
RHA	Radiation Hardness Assurance
SEE	Single Event Effects
SEL	Single Event Latchup
SET	Single Event Transient
TID	Total Ionizing Dose
TMR	Triple Modular Redundancy
CDM	Charged-device Model
HBM	Human-body Model

3 LOGIC DATA

3.1 TRUTH TABLE

The AP54RHC301 truth table is found in Table 1. **H** indicates HIGH logic level, **L** indicates LOW logic level and **X** indicates DON'T CARE. Subscript **n** reflects one of the two functions in the device (1 to 2).

Table 1: AP54RHC301 Device Truth Table

Input			Output	
A_n	B_n	C_n	Y_n	$E_{OUT}n$
L	L	L	L	L
L	L	H	L	H
L	H	L	L	H
L	H	H	H	H
H	L	L	L	H
H	L	H	H	H
H	H	L	H	H
H	H	H	H	L

Input	Internal Voting		Output
E_{IN}	$E_{OUT}1$	$E_{OUT}2$	E_{DET}
L	L	L	L
X	X	H	H
X	H	X	H
H	X	X	H

4 PIN CONFIGURATION

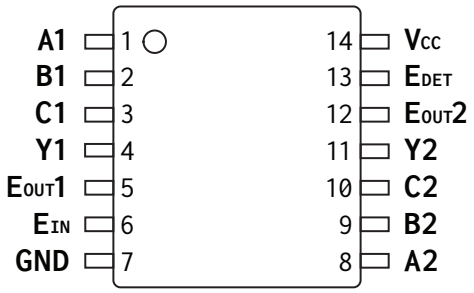


Figure 2: AP54RHC301 Device Pinout

Table 2: AP54RHC301 Device Pinout

PIN NAME(S)	PIN NUMBER(S)	DESCRIPTION
A1, B1, C1 A2, B2, C2	1, 2, 3 8, 9, 10	Logic Inputs
Y1 Y2	4 11	Logic Outputs
E_{IN}	6	External Voter Error Input
$E_{OUT}1$ $E_{OUT}2$	5 12	Internal Voter Error Outputs
E_{DET}	13	Error Detected Output
V_{CC}	14	Positive Voltage Supply
GND	7	Ground

5 ELECTRICAL CHARACTERISTICS

The sign convention for current follows JEDEC standards with negative values representing current sourced from the device and positive values representing current sunk into the device.

5.1 ABSOLUTE MAXIMUM RATINGS

Excursions beyond the values listed in Table 3 may cause permanent damage to the device. Proper function of the device cannot be guaranteed if these values are exceeded, and long-term device reliability may be affected. Functionality of the device at these values, or beyond those listed in Recommended Operating Conditions (Table 4) is not guaranteed.

All parameters are specified across the entire operating temperature range unless otherwise specified.

Table 3: Absolute Maximum Ratings

SYMBOL	PARAMETER		VALUE	UNITS
V_{CC}	Supply Voltage		-0.5 to +5.5	V
V_I	Input voltage range		-0.5 to +5.5	V
V_O	Output voltage range		-0.5 to V_{CC} + 0.5[1]	V
I_{IK} (V_I < 0)	Input clamp current		100	mA
I_O	Continuous output current (per pin)		100	mA
I_{CC}	Maximum supply current		100	mA
V_{ESD}	ESD Voltage	HBM	4000	V
		CDM	500	V
T_J	Operating junction temperature range		-55 to +150	°C
T_{STG}	Storage temperature range		-65 to +150	°C

(1) V_O must remain below absolute maximum rating of V_{CC}

5.2 RECOMMENDED OPERATING CONDITIONS

All recommended parameters below are specified across the entire operating temperature range unless otherwise specified.

Table 4: Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	MAX	UNITS
V_{CC}	Supply voltage		1.65	5.5	V
V_I	Input voltage range		0	5.5	V
V_O	Output voltage range		0	V_{CC}	V
V_{IH}	HIGH-level input voltage	V_{CC} = 1.65 to 1.95 V	1.4	-	V
		V_{CC} = 2.3 to 2.7 V	1.9	-	
		V_{CC} = 3.0 to 3.6 V	2.5	-	
		V_{CC} = 4.5 to 5.5 V	3.8	-	
V_{IL}	LOW-level input voltage	V_{CC} = 1.65 to 1.95 V	-	0.4	V
		V_{CC} = 2.3 to 2.7 V	-	0.6	
		V_{CC} = 3.0 to 3.6 V	-	0.9	
		V_{CC} = 4.5 to 5.5 V	-	1.35	
I_{OH}	HIGH-level output current	V_{CC} = 1.65 to 1.95 V	-	-4	mA
		V_{CC} = 2.3 to 2.7 V	-	-8	
		V_{CC} = 3.0 to 3.6 V	-	-16	
		V_{CC} = 4.5 to 5.5 V	-	-24	
I_{OL}	LOW-level output current	V_{CC} = 1.65 to 1.95 V	-	4	mA
		V_{CC} = 2.3 to 2.7 V	-	8	
		V_{CC} = 3.0 to 3.6 V	-	16	
		V_{CC} = 4.5 to 5.5 V	-	24	
t_r, t_f	Input rise or fall time (10% - 90%)	V_{CC} = 1.65 to 1.95 V	-	1000	ns
		V_{CC} = 2.3 to 2.7 V	-	600	
		V_{CC} = 3.0 to 3.6 V	-	500	
		V_{CC} = 4.5 to 5.5 V	-	400	

Table 5: Thermal Information

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
T_J	Operating junction temperature	-55	-	+125	°C
$R_{\theta JA}$	Junction to ambient thermal resistance	-	100	-	°C/W

5.3 STATIC CHARACTERISTICS

All parameters are specified across the entire operating temperature range unless otherwise specified.

Table 6: DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	V_{CC}	MIN	TYP	MAX	UNITS
V_{OL}	LOW-Level Output Voltage	I_O = 100 µA	1.65 to 5.5 V	-	0.02	0.05	V
		I_O = 1 mA	1.65 to 5.5 V	-	0.05	0.15	V
		I_O = 4 mA	1.65 V	-	0.27	0.8	V
			2.3 V	-	0.3	0.6	V
			3.0 V	-	0.2	0.4	V
			4.5 V	-	0.2	0.4	V
		I_O = 8 mA	2.3 V	-	0.6	1.0	V
			3.0 V	-	0.4	0.8	V
			4.5 V	-	0.3	0.6	V
		I_O = 16 mA	3.0 V	-	1.0	1.4	V
			4.5 V	-	1.1	1.2	V
		I_O = 24 mA	4.5 V	-	1.1	1.5	V
V_{OH}	HIGH-Level Output Voltage	I_O = -100 µA	1.65 to 5.5 V	V_{CC} - 0.1	V_{CC} - 0.02	-	V
		I_O = -1 mA	1.65 to 5.5 V	V_{CC} - 0.15	V_{CC} - 0.08	-	V
		I_O = -4 mA	1.65 V	1	1.35	-	V
			2.3 V	1.8	2.0	-	V
			3.0 V	2.6	2.8	-	V
			4.5 V	4.2	4.4	-	V
		I_O = -8 mA	2.3 V	1.4	1.7	-	V
			3.0 V	2.2	2.5	-	V
			4.5 V	3.9	4.1	-	V
		I_O = -16 mA	3.0 V	1.5	2.0	-	V
			4.5 V	3.3	3.8	-	V
		I_O = -24 mA	4.5 V	3.0	3.5	-	V
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND I_O = 0 mA	5.5 V	-	125	205	µA
I_I	Input current	V_I = V_{CC} or GND	1.65 to 5.5 V	-	-	±1	µA
I_{OFF}	Powerdown leakage current[1]	V_I = V_{CC} or GND	OFF[2]	-	-	5	µA

[1] into any input or output port
[2] V_{CC} is at GND potential

5.4 DYNAMIC CHARACTERISTICS

All parameters are specified across the entire operating temperature range unless otherwise specified.

Table 7: AC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	V_{CC}	MIN	TYP	MAX	UNITS
t_{pd}[1]	Propagation Delay (Input A_n, B_n or C_n to Output Y_n)	C_L = 50 pF	4.5 to 5.5 V	-	6.1	11	ns
			3.0 to 3.6 V	-	7.6	13	ns
			2.3 to 2.7 V	-	9.5	15	ns
			1.65 to 1.95 V	-	13.8	25	ns
t_{err_det}	Propagation Delay (Input A_n, B_n or C_n to Output $E_{OUT}n$)	C_L = 50 pF	4.5 to 5.5 V	-	8.5	16	ns
			3.0 to 3.6 V	-	10.8	21	ns
			2.3 to 2.7 V	-	13.7	24	ns
			1.65 to 1.95 V	-	20.3	35	ns
t_{pd_err}	Propagation Delay (Input E_{IN} to Output E_{DET})	C_L = 50 pF	4.5 to 5.5 V	-	5.6	11	ns
			3.0 to 3.6 V	-	6.9	13	ns
			2.3 to 2.7 V	-	8.8	15	ns
			1.65 to 1.95 V	-	12.8	25	ns
C_{in}	Input Capacitance[2]	V_I = V_{CC} or GND	1.65 to 5.5 V	-	2	4	pF
C_{pd}	Power Dissipation Capacitance[2]	I_O = 0 mA f = 1 MHz	5.5 V	-	40	-	pF

(1) equivalent to t_{PLH}, t_{PHL}
(2) guaranteed by design

5.5 RADIATION RESILIENCE

For detailed radiation testing reports, please contact Apogee Semiconductor at sales@apogeesemi.com.

Table 8: Radiation Resilience Characteristics

PARAMETER	CONDITIONS	VALUE	UNITS
Total Ionizing Dose (TID)	Please contact Apogee Semiconductor for test report.	30	krad (Si)
SEL Onset LET Threshold	Please contact Apogee Semiconductor for test report.	≥80	MeV-cm^2/mg

5.6 CHARACTERISTICS MEASUREMENT INFORMATION

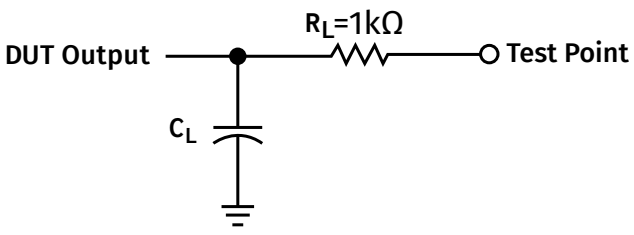


Figure 3: Load Circuit

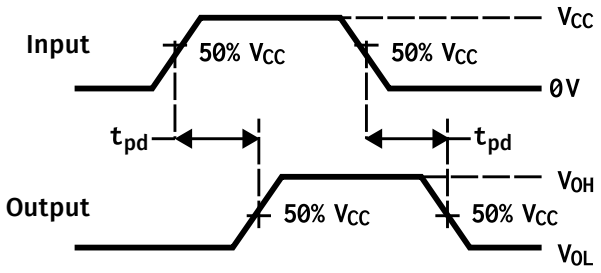


Figure 4: Propagation Delay Measurement

6 DETAILED DESCRIPTION

The AP54RHC301 is a dual three-input majority voter gate that that offers two instances of a triple-input voter gate, with individual error outputs, a dedicated “error detected” output, and an external error signal input. Designed to operate from a wide supply voltage of 1.65 to 5.5 V, it has fully redundant input and output stages providing for superior resiliency to single event effects.

The output and input stages are constructed with transient-activated clamps (Figure 5, 6) that prevent inadvertent biasing of the V_{CC} power rail through parasitic diodes inherent to conventional input, output, and ESD circuits. The IC also incorporates an internal power-on reset (POR) circuit that prevents the output from driving erroneous results during power-on, and guarantees correct operation at power supply voltages as low as 1.65 V. While the supply is ramping, the POR holds the output buffer in tri-state, a feature that prevents unwanted DC current during cold sparing on input and output pins.

The AP54RHC family’s I/O protection circuitry allows for cold sparing configurations as it avoids a leakage current penalty on inputs and outputs while in a power-down state. This can result in considerable power savings in systems where multiple-path redundancy is employed. The ESD clamp circuits for this logic family are designed to support Class 2 ESD levels of 4 kV HBM and 500 V CDM.

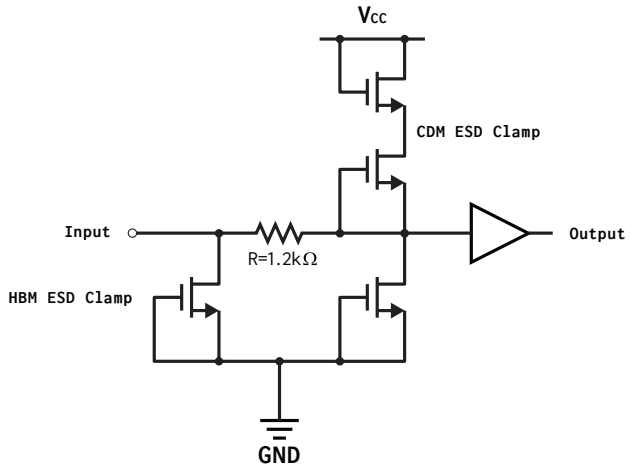


Figure 5: Input Pin Structure

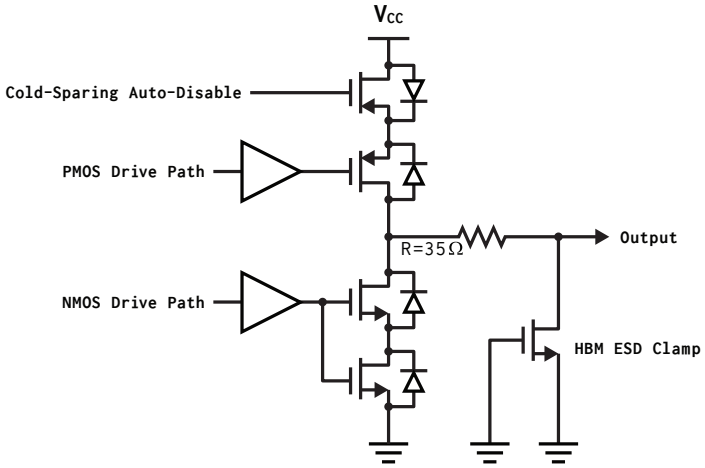


Figure 6: Output Pin Structure

7 APPLICATIONS INFORMATION

The voter function of the AP54RHC301 is intended to allow fault-free glitchless operation in logic systems employing triple redundancy, e.g. where specific logic functions are triplicated and all three identical functions are simultaneously active (Figure 7). This may be simple discrete logic that serves a specific purpose, or complex microcontroller-based logic that is responsible for multiple data-processing and control functions.

The three identical blocks are assumed to perform the same operation, share the same stimuli, and produce the same result at a given single-bit output (e.g., an on/off control line that turns on a valve). These three results are compared by the voter to make sure that they are in agreement.

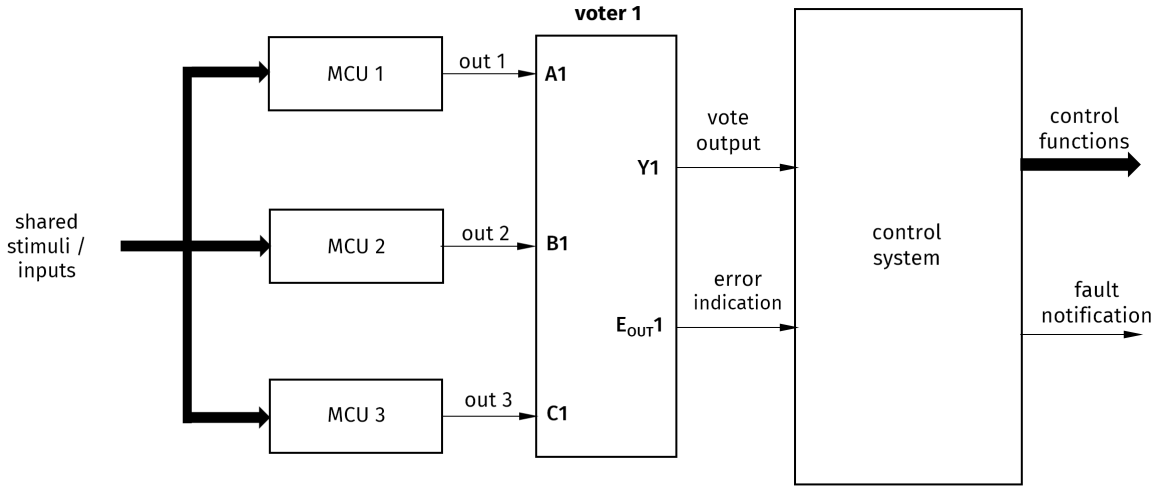


Figure 7: Voter Example

When only two of them are in agreement and the third one is not, the voter's output will produce the result of a majority vote (Y_n), which assumes that a fault has occurred in the single function whose output did not agree with that of the other two. Alongside the vote result, the voter will also produce an error signal ($E_{OUT}n$), which may be used to produce a fault notification.

This fault may be either the result of permanent damage in that function, or may be the consequence of a SEE, in which case there is a chance that the block will return to normal functionality and the error indication will be reset. The AP54RHC301 contains two instances of this voting function.

7.1 APPLICATIONS EXAMPLE

As the AP54RHC family is radiation-hardened by design and includes internal TMR, it can be utilized in high-reliablity applications without additional supporting circuitry or devices. Nonetheless, some application requirements call for fully-redundant designs, where an "A" and a "B" device are required, often on separate power rails.

With the cold sparing capability of the AP54RHC family, fully redundant "A" and "B" functions may be placed in parallel (as seen in Figure 8) running off redundant power supplies. The inputs and outputs on each one of these functions are assumed to be based on the AP54RHC family, allowing for direct parallel connection without unwanted leakage current paths during cold sparing. In the event of a failure in power supply A or within function A, the system can simply shut power supply A off and switch on power supply B, without requiring additional input or output switching or configuration changes.

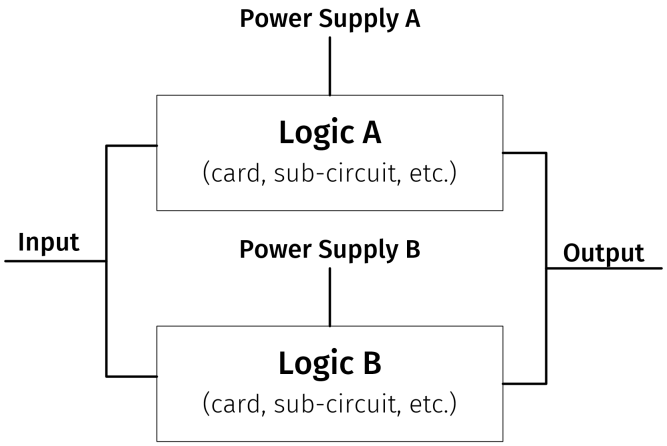


Figure 8: Two-Path Cold-Sparing Configuration

7.2 POWER SUPPLY RECOMMENDATIONS

This device can operate at any voltage within the range specified in Table 4 Recommended Operating Conditions.

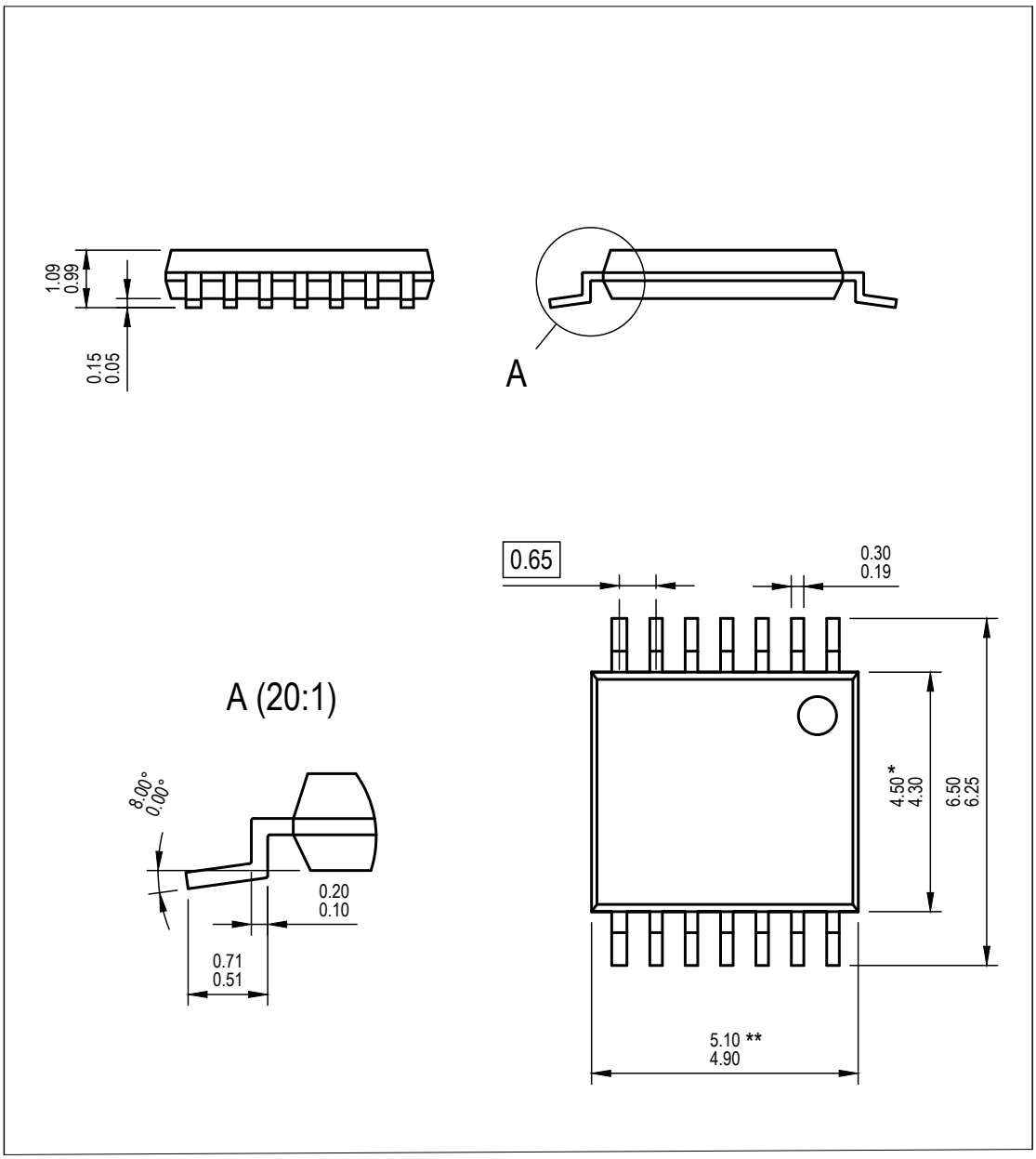
At a minimum, a 16 VDC (or higher), X7R-rated 0.1 µF ceramic decoupling capacitor should be placed near (within 1 cm) the V_{CC} pin of the device.

7.3 APPLICATION TIPS

Unused **inputs** must **not** be left floating. They may be connected to either a low (GND) or high (V_{CC}) bias to provide a known state at the input of the device. Resistors may be used to tie off unused inputs. In the event of a design change, such resistors can be removed, thereby allowing use of the inputs without having to cut traces on the PCB.

An unused **output** may be left floating. It is suggested that it be routed to a test point or similar accessible structure in case the gate needs to be utilized as part of a design revision.

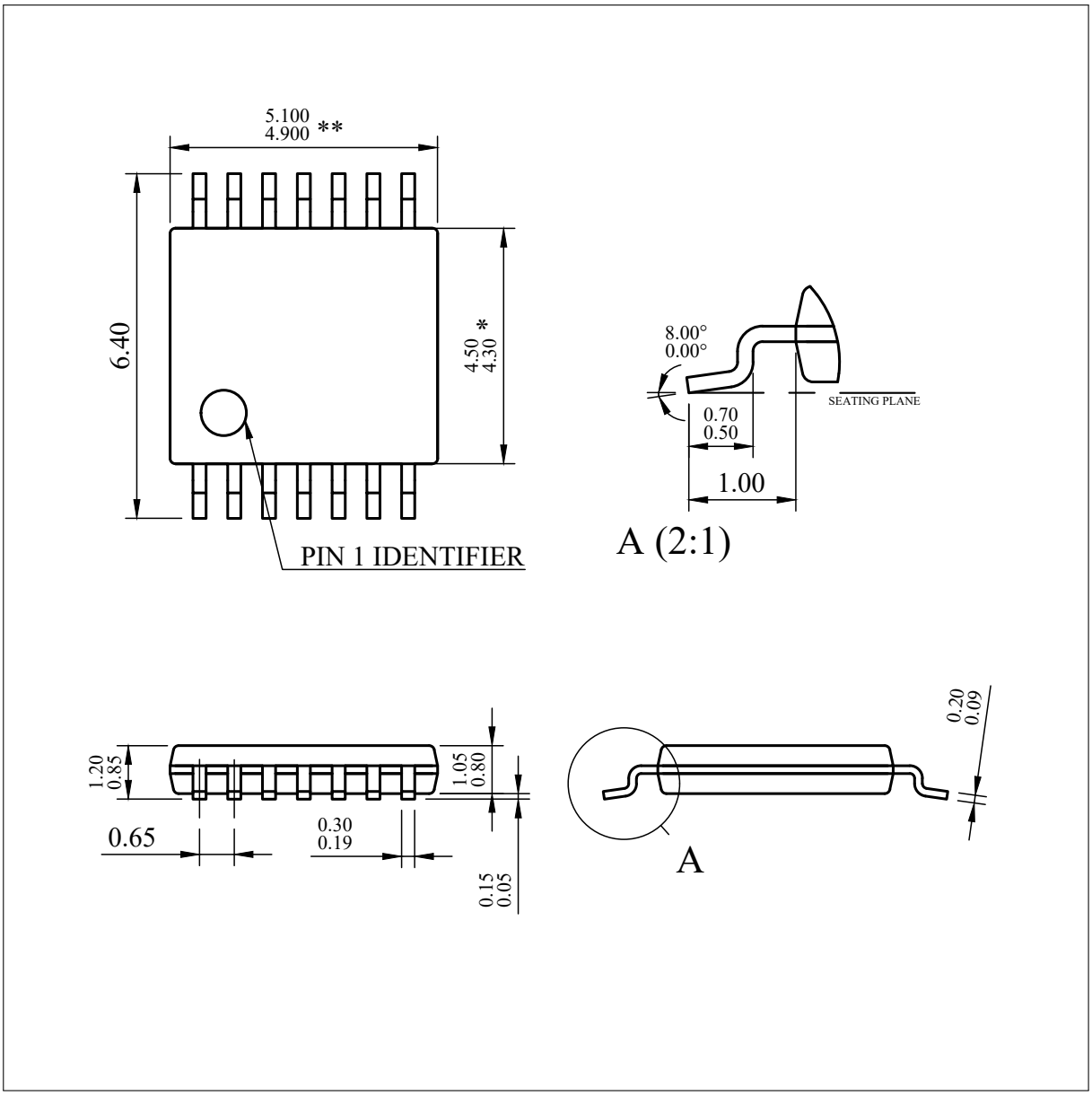
8 PACKAGING INFORMATION



Notes:
1. All linear dimensions are in millimeters. Dimensioning and tolerancing are as per ISO/TS 128-71:2010
2. The part is compliant with JEDEC MO-153 specifications.

* Body width does **not** include interlead flash. Interlead flash shall not exceed 0.25 mm each side.
** Body length does **not** include mold flash, protrusion, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0.15 mm on each side.

Figure 9: 14-LT - Package Mechanical Drawing (SnPb)



Notes:
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* Body width does **not** include interlead flash. Interlead flash shall not exceed 0.25 mm each side.
** Body length does **not** include mold flash, protrusion, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0.15 mm on each side.

Figure 10: 14-NT - Package Mechanical Drawing (NiPdAu)

9 ORDERING INFORMATION

Example part numbers for the AP54RHC301 are listed in Table 9. The full list of options for this part can be found in Figure 11. For a detailed description of product grades, please refer to Product Grades and Quality Flows document. Please contact Apogee Semiconductor sales at sales@apogeesemi.com for further information on sampling, lead time and purchasing on specific part numbers.

Table 9: AP54RHC301 Ordering Information

DEVICE	DESCRIPTION	PACKAGE	LEAD FINISH	PACKAGE DIAGRAM	PACKAGE MASS
AP54RHC301ALT-R	Rad-Hard Dual 3-Input Majority Voter (30 krad (Si))	TSSOP-14	SnPb	14-LT	47 mg
AP54RHC301ALT-J(1)	Rad-Hard Dual 3-Input Majority Voter (30 krad (Si))	TSSOP-14	SnPb	14-LT	47 mg
AP54RHC301BLT-R	Rad-Hard Dual 3-Input Majority Voter (30 krad (Si))	TSSOP-14	SnPb	14-LT	47 mg
AP54RHC301BLT-J(1)	Rad-Hard Dual 3-Input Majority Voter (30 krad (Si))	TSSOP-14	SnPb	14-LT	47 mg
AP54RHC301CLT-R	Rad-Hard Dual 3-Input Majority Voter (30 krad (Si))	TSSOP-14	SnPb	14-LT	47 mg
AP54RHC301CLT-J(1)	Rad-Hard Dual 3-Input Majority Voter (30 krad (Si))	TSSOP-14	SnPb	14-LT	47 mg
AP54RHC301ELT-R	Rad-Hard Dual 3-Input Majority Voter (for eval only)	TSSOP-14	SnPb	14-LT	47 mg
AP54RHC301ELT-J(1)	Rad-Hard Dual 3-Input Majority Voter (for eval only)	TSSOP-14	SnPb	14-LT	47 mg
AP54RHC301ANT-R	Rad-Hard Dual 3-Input Majority Voter (30 krad (Si))	TSSOP-14	NiPdAu	14-NT	58 mg
AP54RHC301ANT-J(1)	Rad-Hard Dual 3-Input Majority Voter (30 krad (Si))	TSSOP-14	NiPdAu	14-NT	58 mg
AP54RHC301BNT-R	Rad-Hard Dual 3-Input Majority Voter (30 krad (Si))	TSSOP-14	NiPdAu	14-NT	58 mg
AP54RHC301BNT-J(1)	Rad-Hard Dual 3-Input Majority Voter (30 krad (Si))	TSSOP-14	NiPdAu	14-NT	58 mg
AP54RHC301CNT-R	Rad-Hard Dual 3-Input Majority Voter (30 krad (Si))	TSSOP-14	NiPdAu	14-NT	58 mg
AP54RHC301CNT-J(1)	Rad-Hard Dual 3-Input Majority Voter (30 krad (Si))	TSSOP-14	NiPdAu	14-NT	58 mg
AP54RHC301ENT-R	Rad-Hard Dual 3-Input Majority Voter (for eval only)	TSSOP-14	NiPdAu	14-NT	58 mg
AP54RHC301ENT-J(1)	Rad-Hard Dual 3-Input Majority Voter (for eval only)	TSSOP-14	NiPdAu	14-NT	58 mg

(1) Available through distributors only.

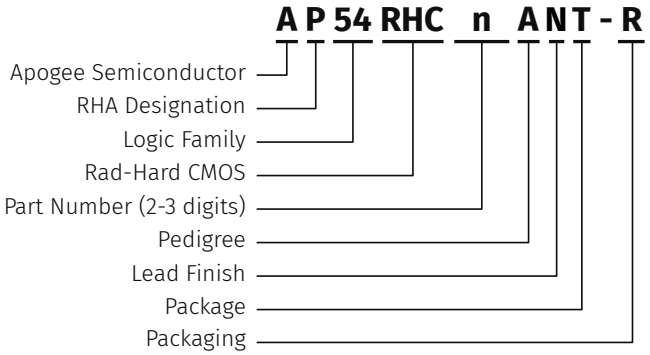

Figure 11: Part Number Decoder

1. RHA Designation
   - **P** 30 krad (Si)
   - **F** 300 krad (Si)
2. Part Number
   - **_** 301 (Dual 3-Input Majority Voter)
3. Pedigree
   - **A** -55 to +125 °C (Burn-in)
   - **B** -55 to +125 °C (No burn-in)
   - **C** 25 °C (No burn-in)
   - **E** 25 °C Functional Test Only (Evaluation)
4. Lead Finish
   - **L** Tin-Lead (SnPb)
   - **N** Nickel-Palladium-Gold (NiPdAu)
5. Package
   - **T** 14-pin Thin Shrink Small Outline Package (TSSOP)
6. Packaging
   - **R** Tape and Reel[1]
   - **J** JEDEC Tray

[1] Contact us for custom reel quantities. Orders less than full reel quantities may be shipped as cut tape.

10 REVISION HISTORY

Table 10: Revision History

REVISION	DESCRIPTION	DATE
A09	Added outgassing feature bullet. Added package mass. Updated description. Updated typicals for AC (table 7). Updated ordering information.	2025-08-14
A08	Fixed typographical error in pinout table. Updated figures 3 and 4 in Characteristics Measurement Information. Add NiPdAu option.	2024-07-19
A07	Correct output pin structure diagram.	2021-12-06
A06	Updated ordering information.	2021-07-30
A05	Updated dynamic characteristics values.	2021-07-17
A04	Correct pin mappings in logic diagram.	2021-06-17
A03	Revamped static and dynamic characteristics with new test data.	2021-02-24
A02	Update Static and Dynamic characteristics.	2020-10-23
A01	Initial public release.	2020-02-29
A00	Initial internal release.	2019-07-05

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